Table of Content

MCIMX7D-SABRE

Revision History

Rev. Code	Date	Description
B	22/09/2015	Initial Draft
B1	21/01/2016	- Changed Q8 from 2N7002 to MMBT3904. - Reconnection U43 SW with the anode of D25. - DNP the capacitor:C6,C121. - Changed the power of JTAG from PERI_3V3 to VLDO3_3V3. - PCIe DNP the resistor:R605,R606,R607,R608. Changed C442 and C443 to 0ohm resistor (R632,R633). Add 49.9 1% 0402 resistors (R634,R635) on PCIE_REFCLKOUT_P/N to GND. - Add the mosfet Q36 on the NET "CSI_PWDN". - Add blocking capacitor(C458,C459) before the terminal reisistor. - Add Schottky diode(D26) to isolate POR_B with JTAG interface. - Use the LDO U44 instead of Q11. - Add the 0ohm resistor(R641) connect the pin CCM_CLK2 to GND. - Add the U45 to match electrical level.
C	28/01/2016	- Changed the revision from "B1" to "C". - Delete the capacitors C312 and C314. - Add several GND test points TP68--TP75 around the DDR3. - Changed connectors type of the J29&J30
D	09/03/2016	- Changed the revision from "C" to "D". - Corrected the PCB decal of the Q8. - Changed connection of the J20.

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Multimedia Application Division,
Wireless & Mobile System Group

ICAP Classification: FCP: FIUO: PUBI:

Designer:	Drawing Title: MCIMX7D-SABRE	
Drawn by:	Page Title: 01 Title Sheet	
Approved: <Approver>	Size A2	Document Number SOURCE:SCH-28590:SPF-28590 Rev D
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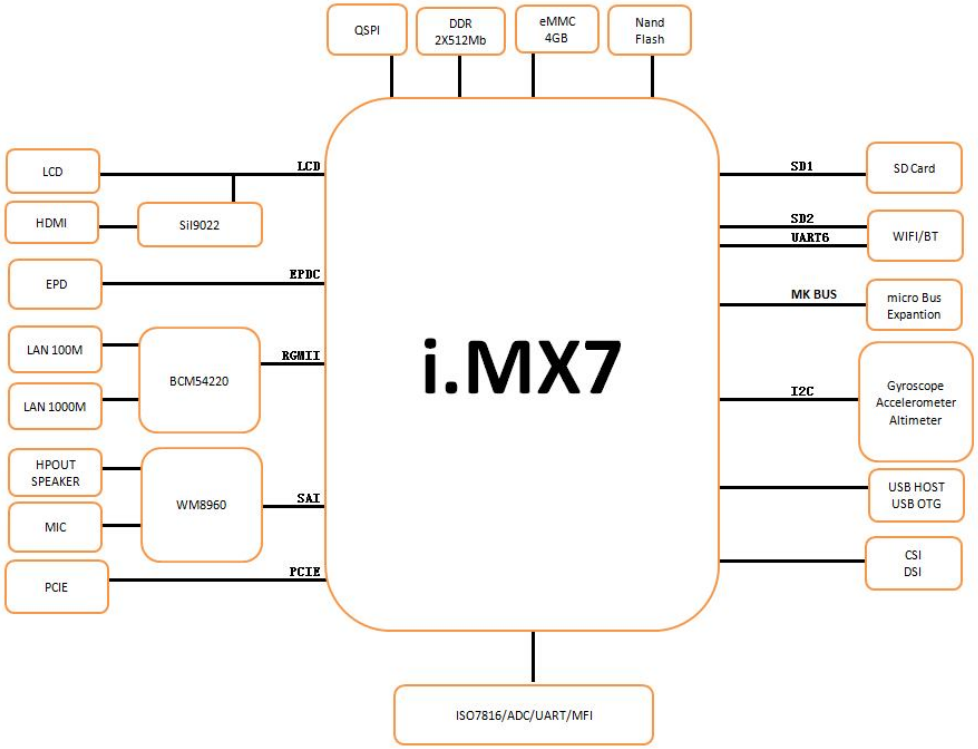
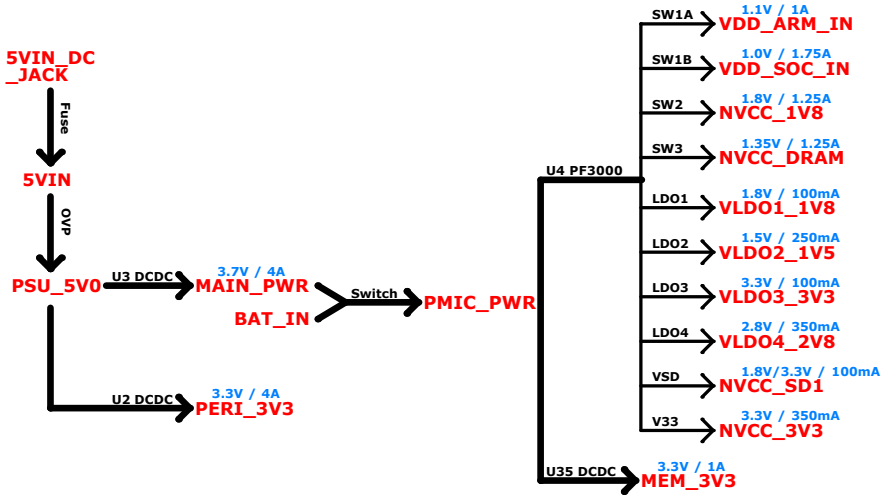
MCIMX7D-SABRE Block Diagram



Power Distribution Diagram



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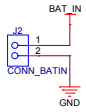
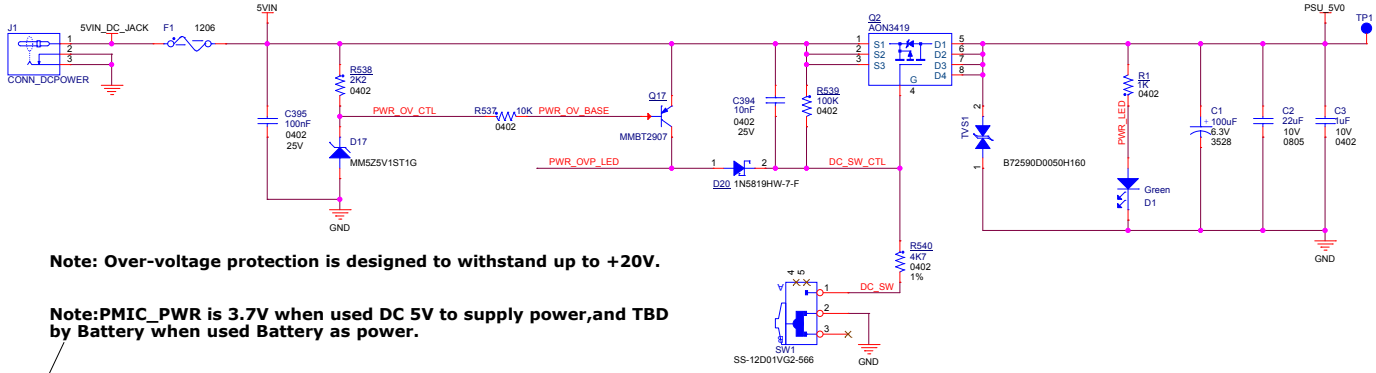
BATTERY IN



5V DC POWER

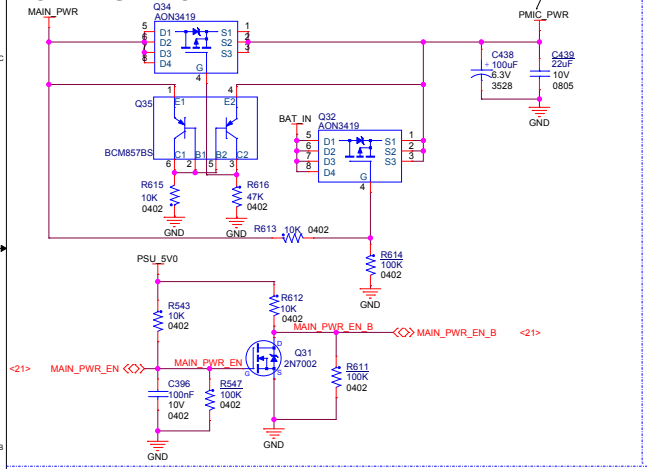
OVER VOLTAGE PROTECTION



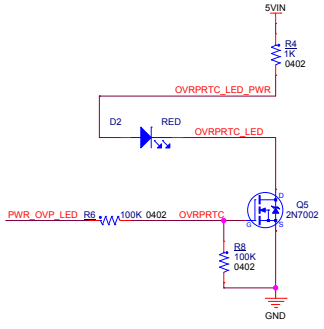
Note: Over-voltage protection is designed to withstand up to +20V.

Note:PMIC_PWR is 3.7V when used DC 5V to supply power,and TBD by Battery when used Battery as power.

POWER SWITCH

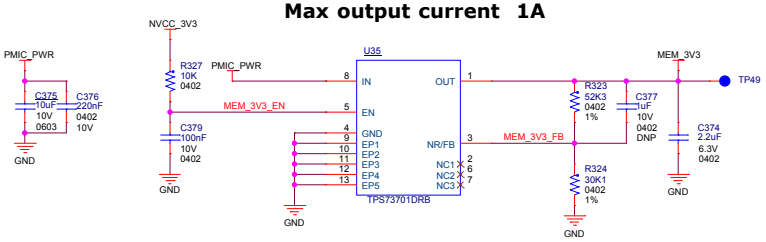


OVER VOLTAGE INTICATOR



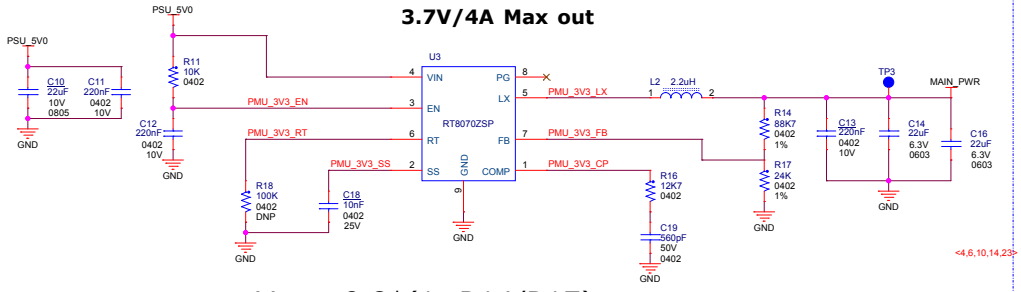
MEM_3V3

Max output current 1A



PMIC POWER IN

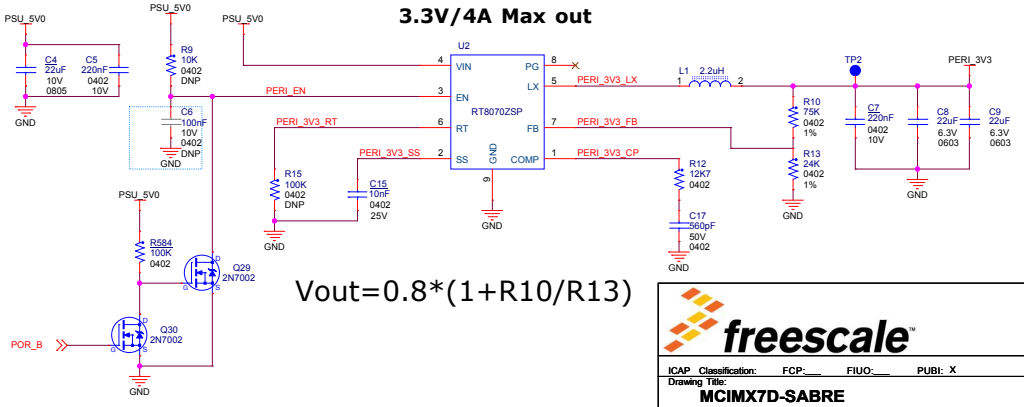
3.7V/4A Max out



Vout=0.8*(1+R14/R17)

3V3 PERI

3.3V/4A Max out



Vout=0.8*(1+R10/R13)

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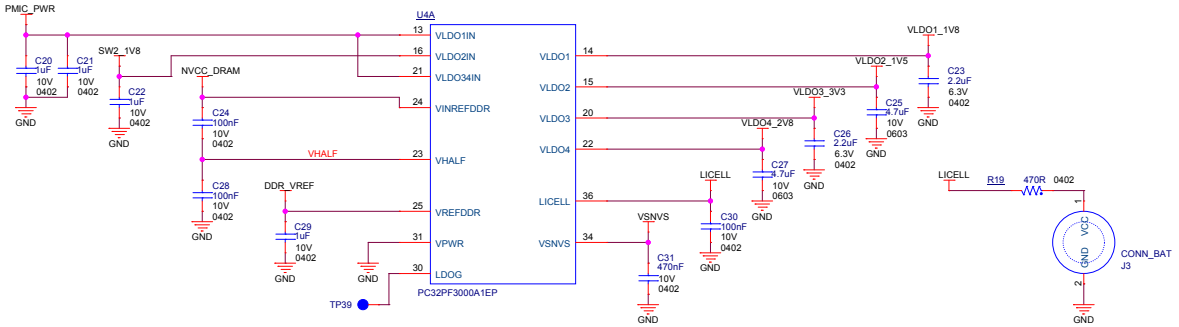
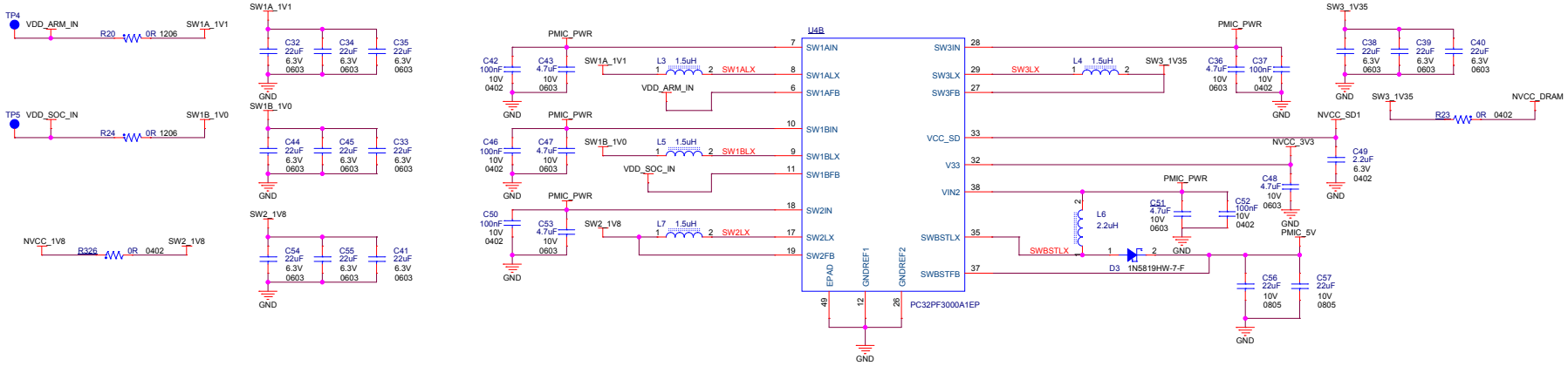
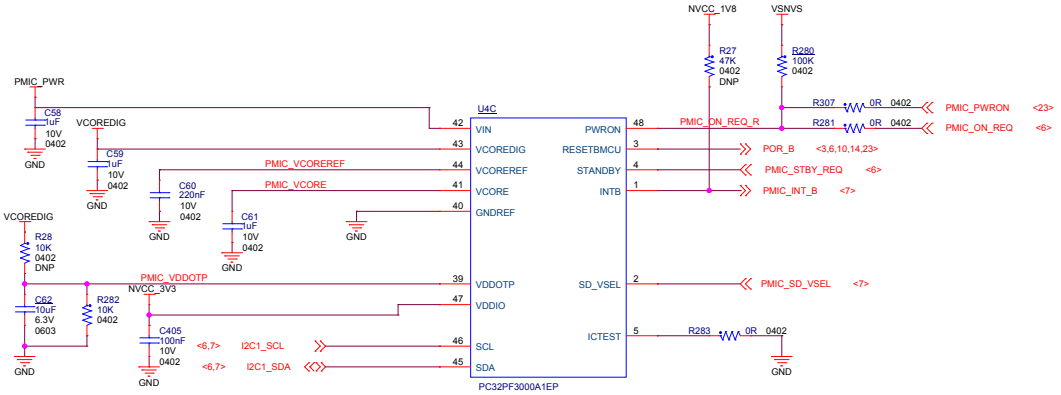
PMIC







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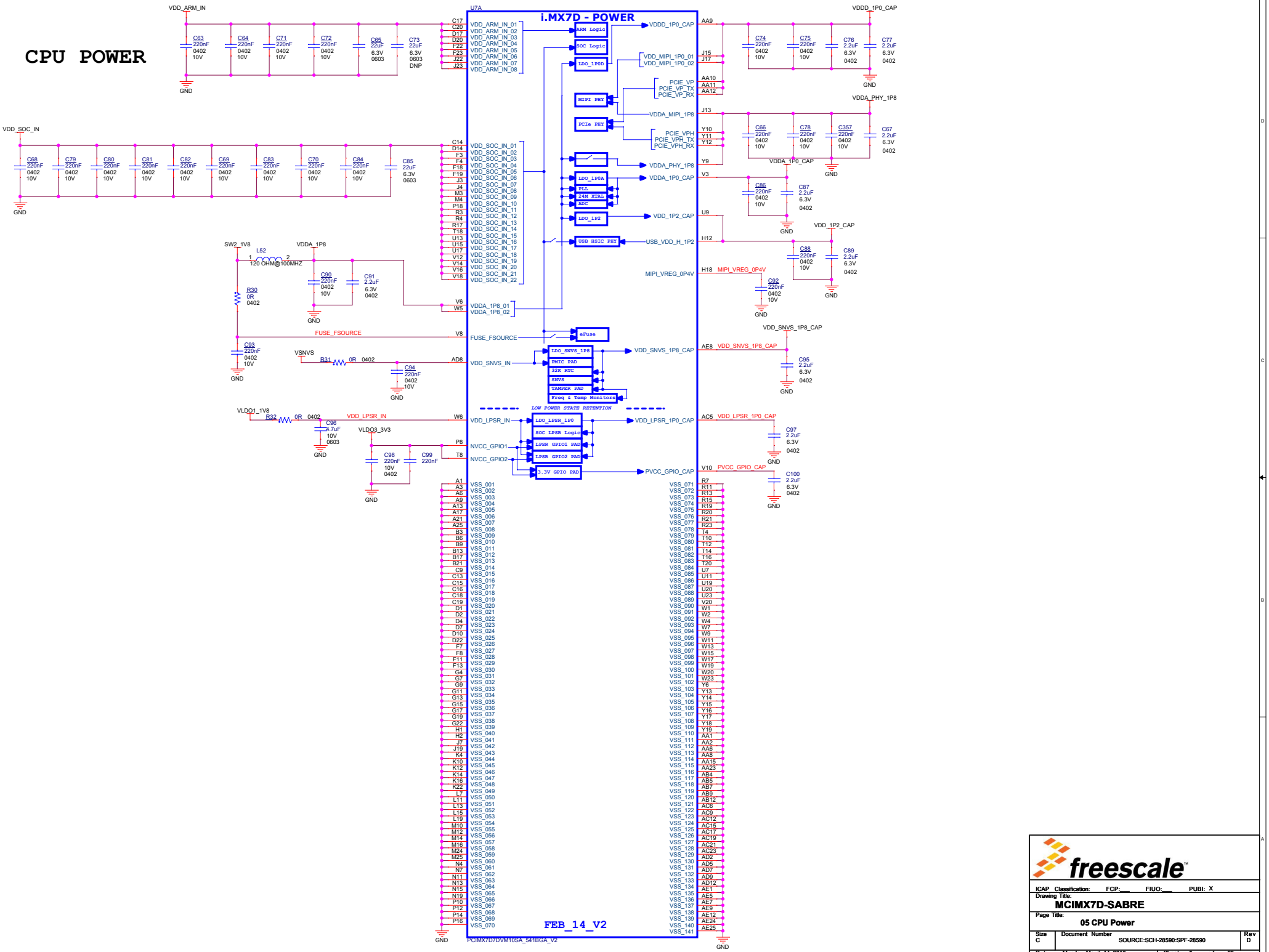
CPU POWER



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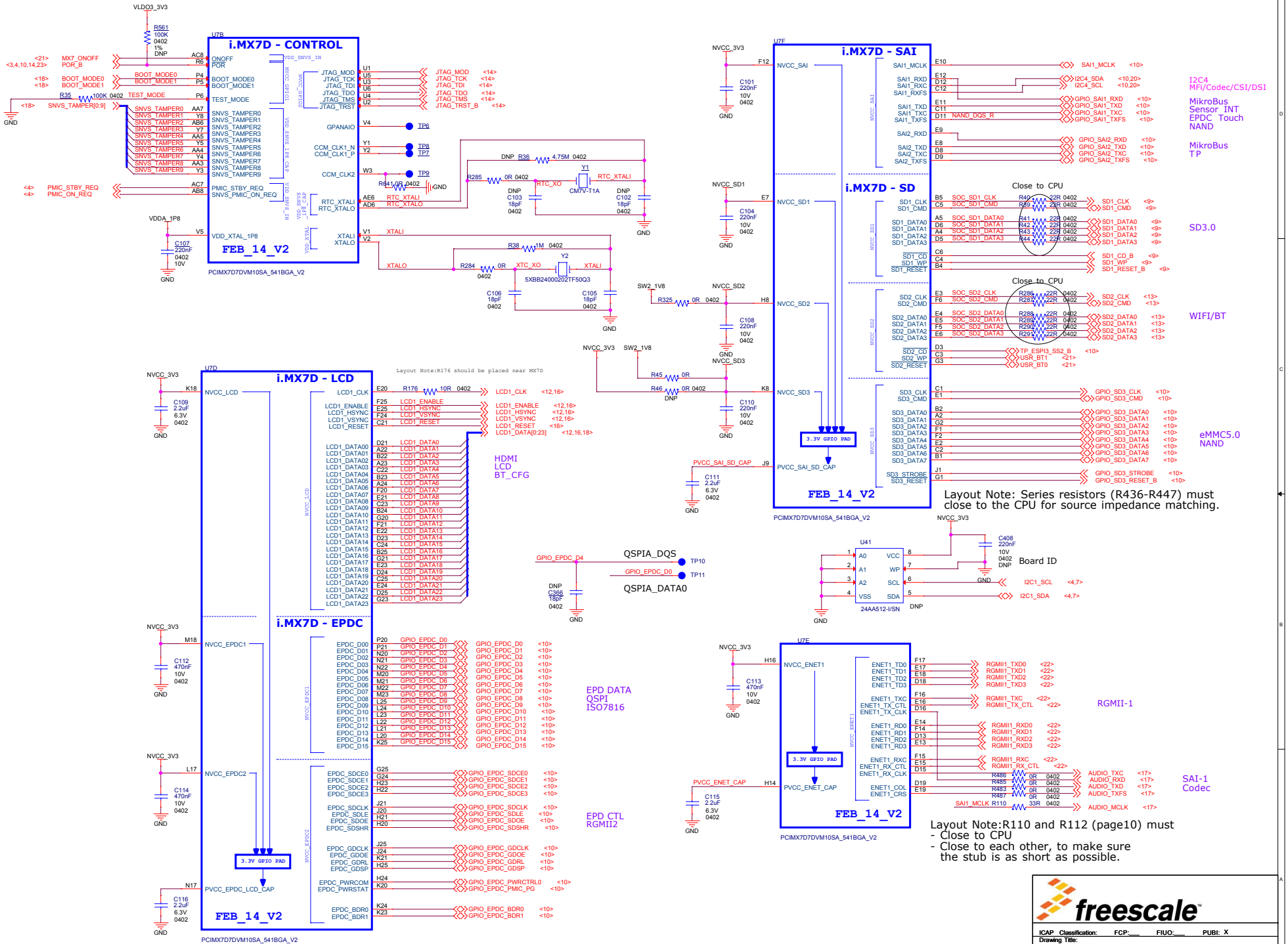

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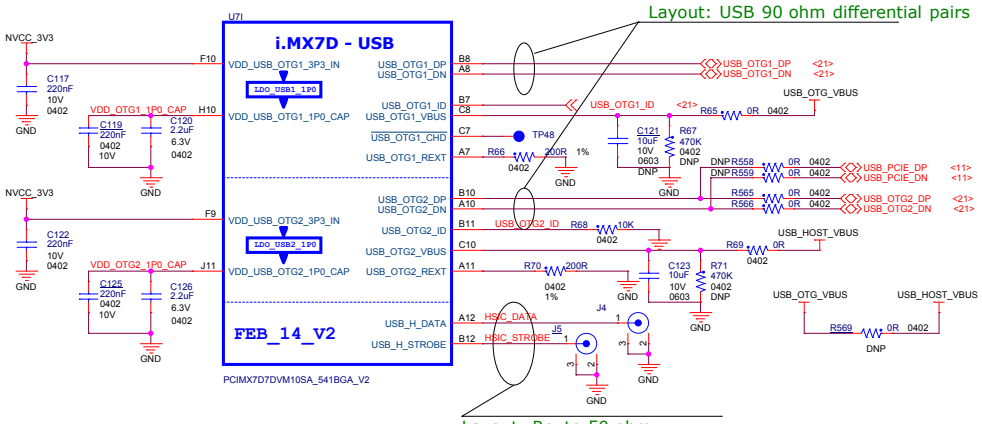

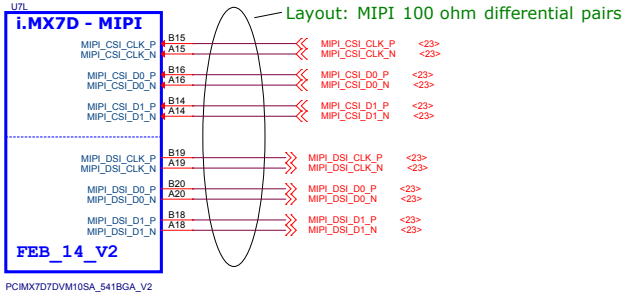

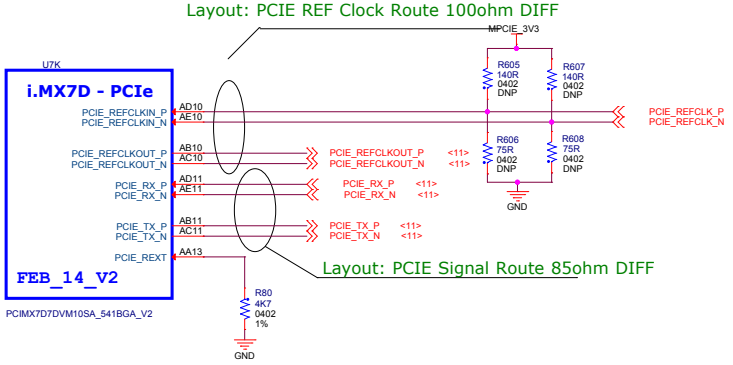

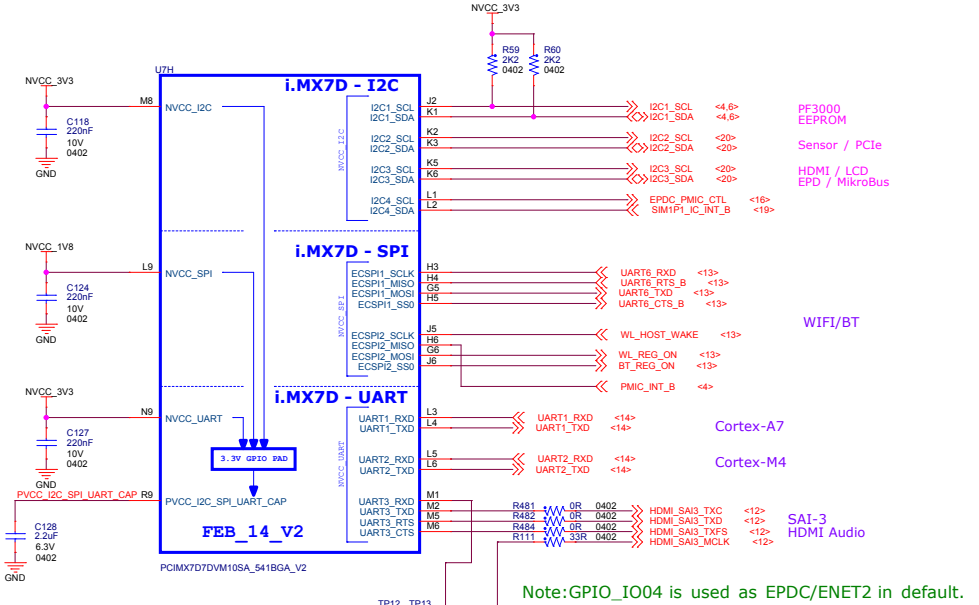

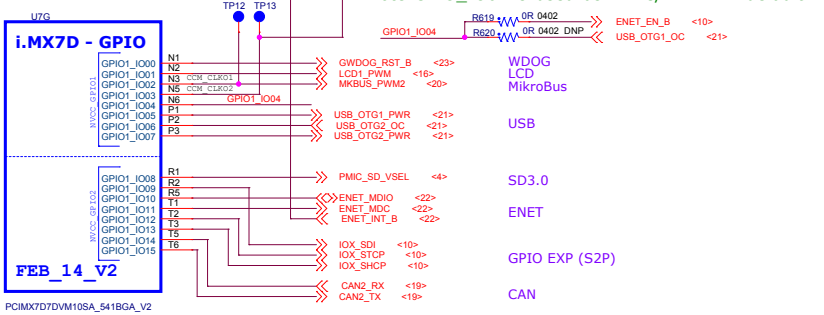

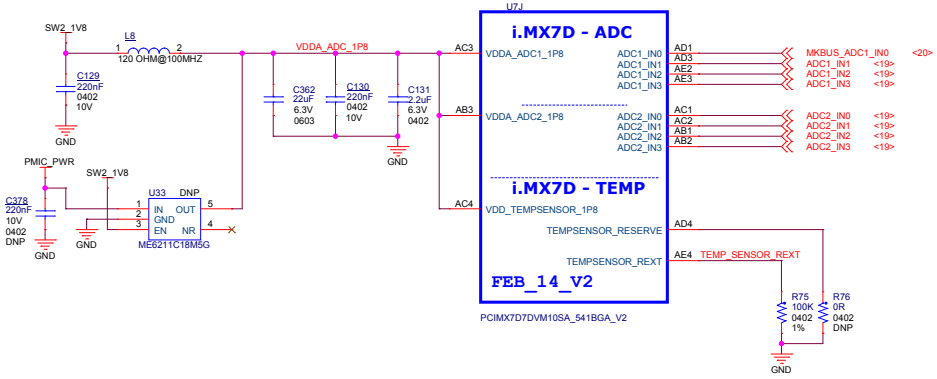

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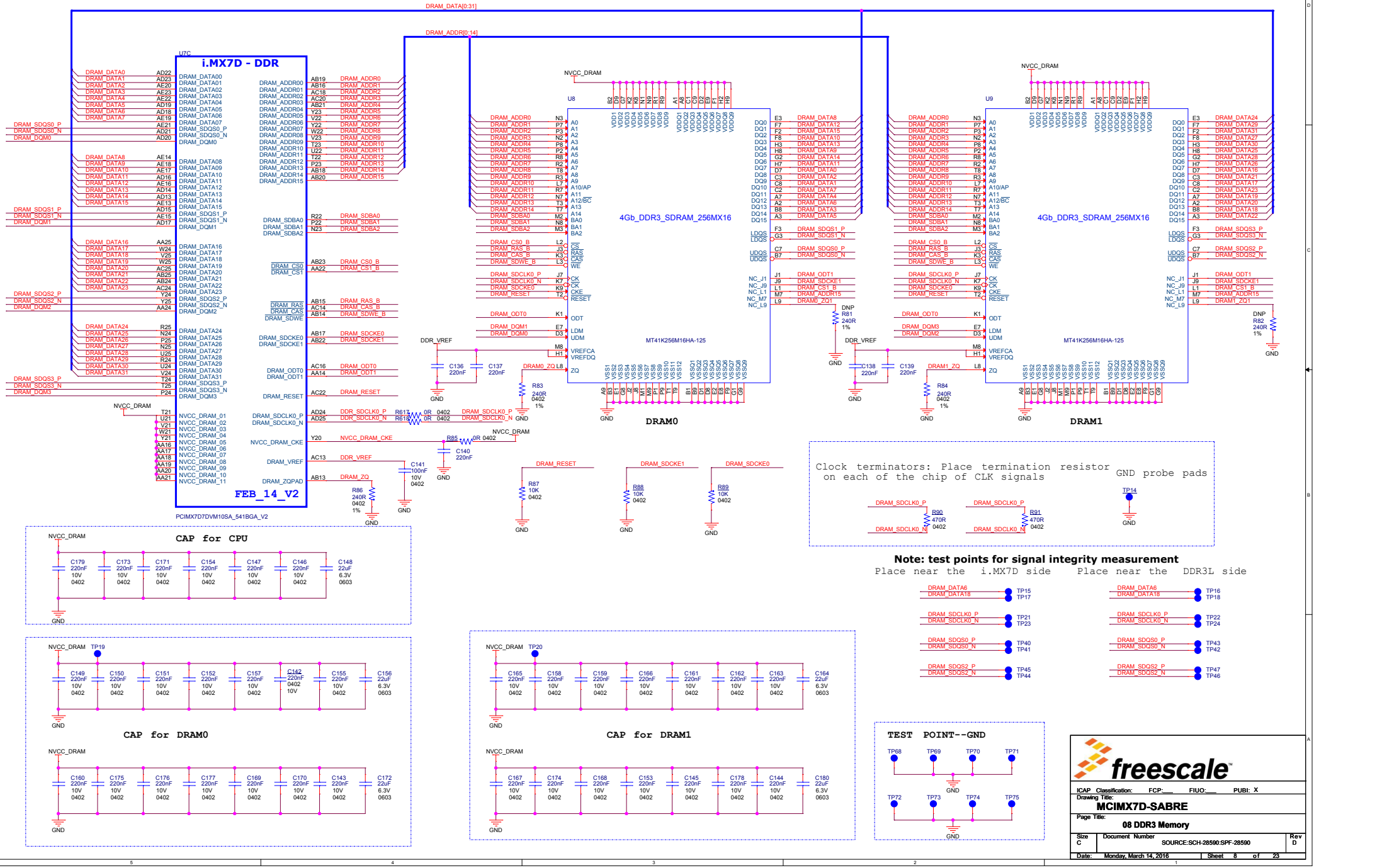
DDR



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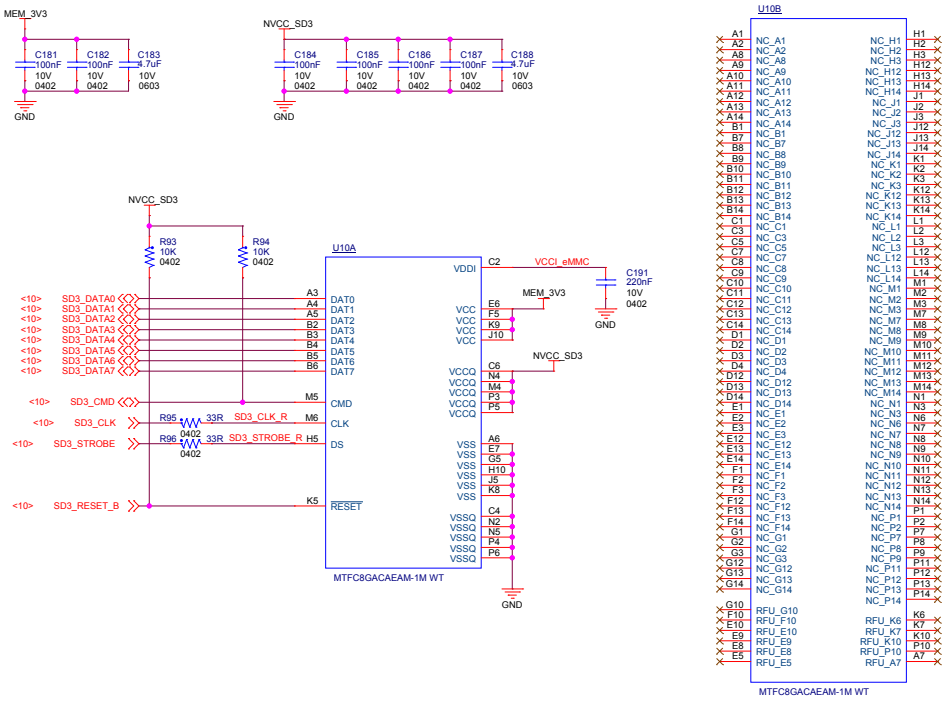
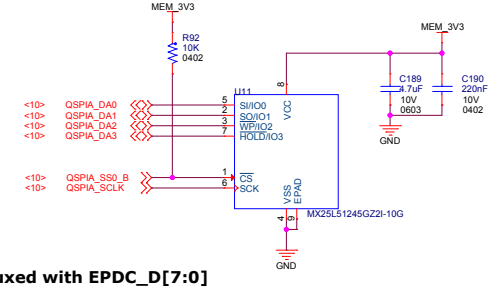
eMMC 5.0

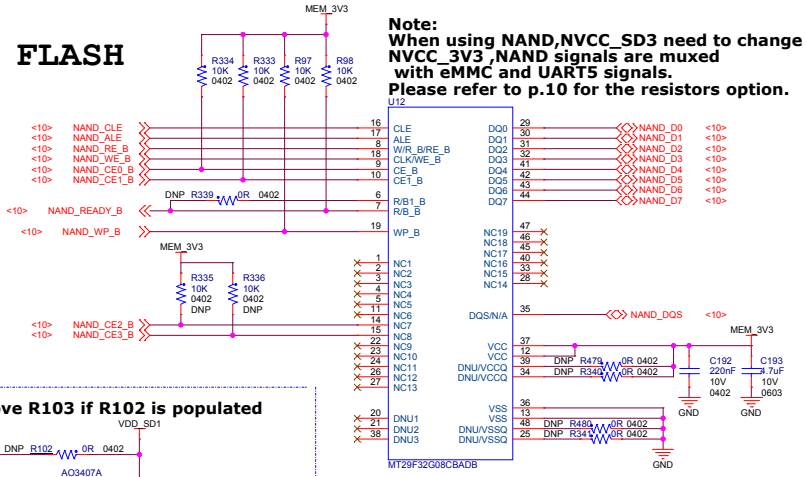


QSPI NOR FLASH



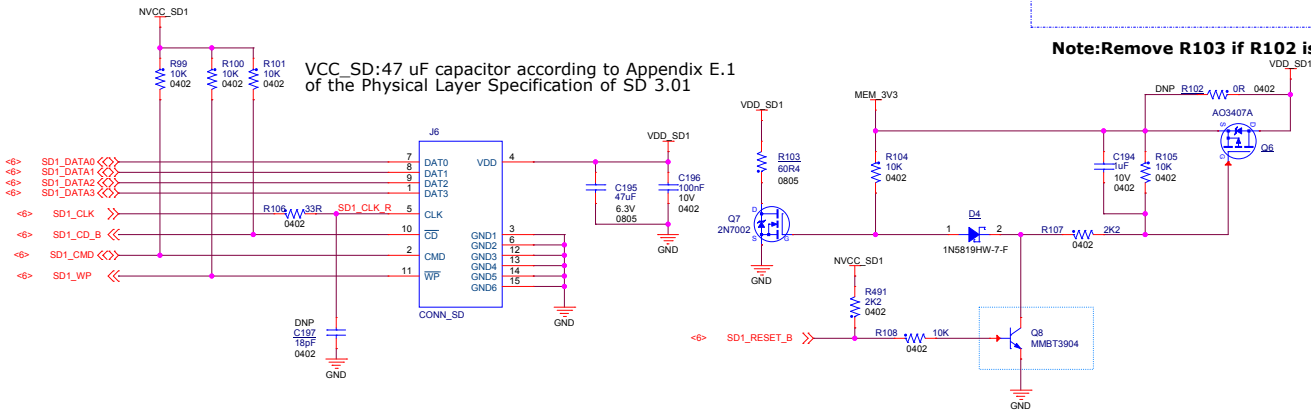
Note:
QSPI signals are muxed with EPDC_D[7:0]
When using QSPI:
de-populate R388-R391, R396-R399
populate R392-R395, R299, R300

NAND FLASH



Note:
When using NAND,NVCC_SD3 need to change to NVCC_3V3 ,NAND signals are muxed with eMMC and UART5 signals.
Please refer to p.10 for the resistors option.

SD CARD



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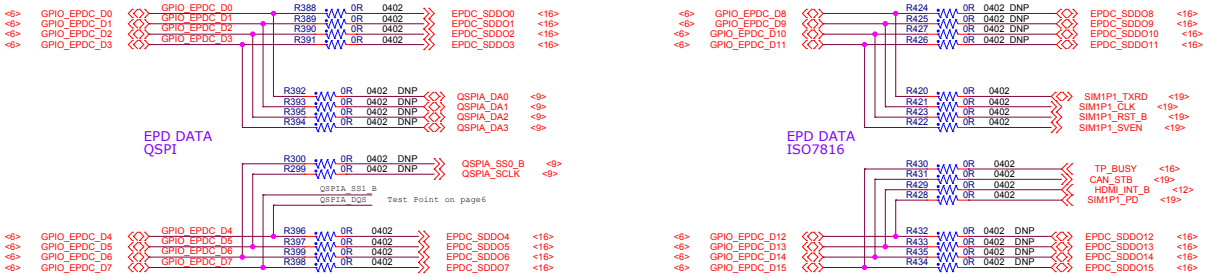
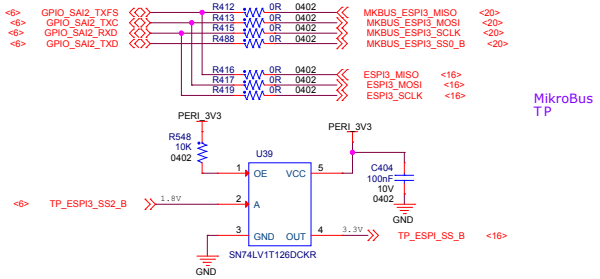
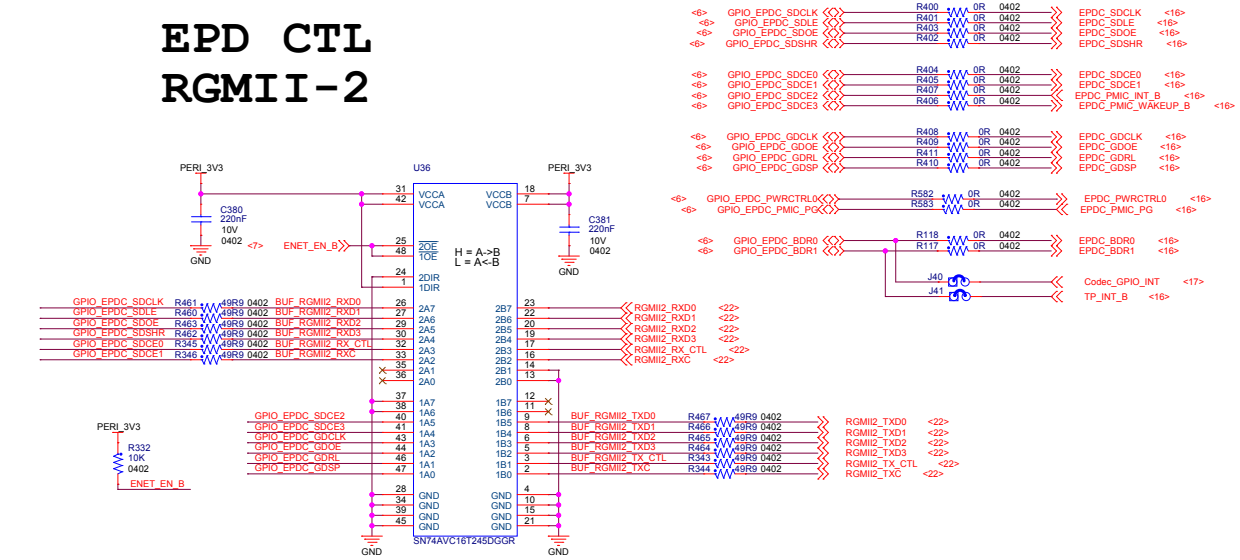
EPD PIN MUX



SAI2 PIN MUX

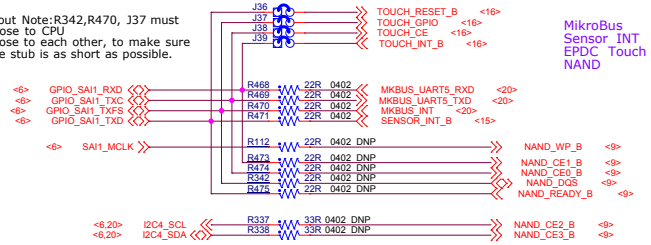


EPD CTL RGMII-2



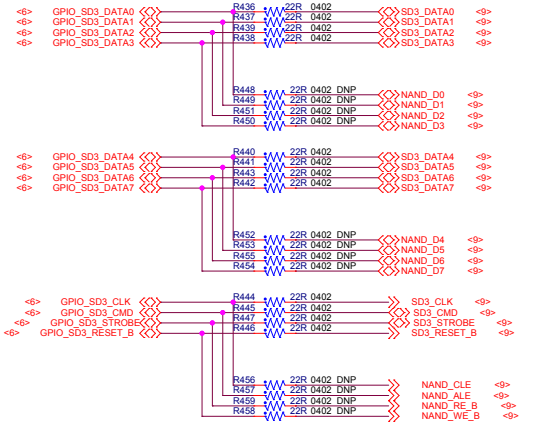
SAI1 PIN MUX

Layout Note:R342,R470, J37 must
- Close to CPU
- Close to each other, to make sure the stub is as short as possible.

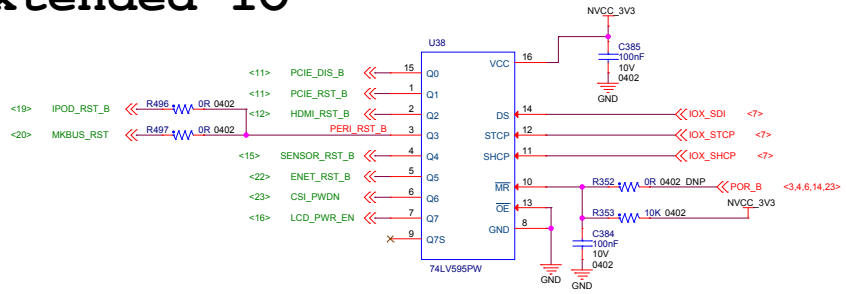


SD3/NAND PIN MUX

Layout Note:NAND and SD resistor must close to the CPU for source impedance matching



Extended IO



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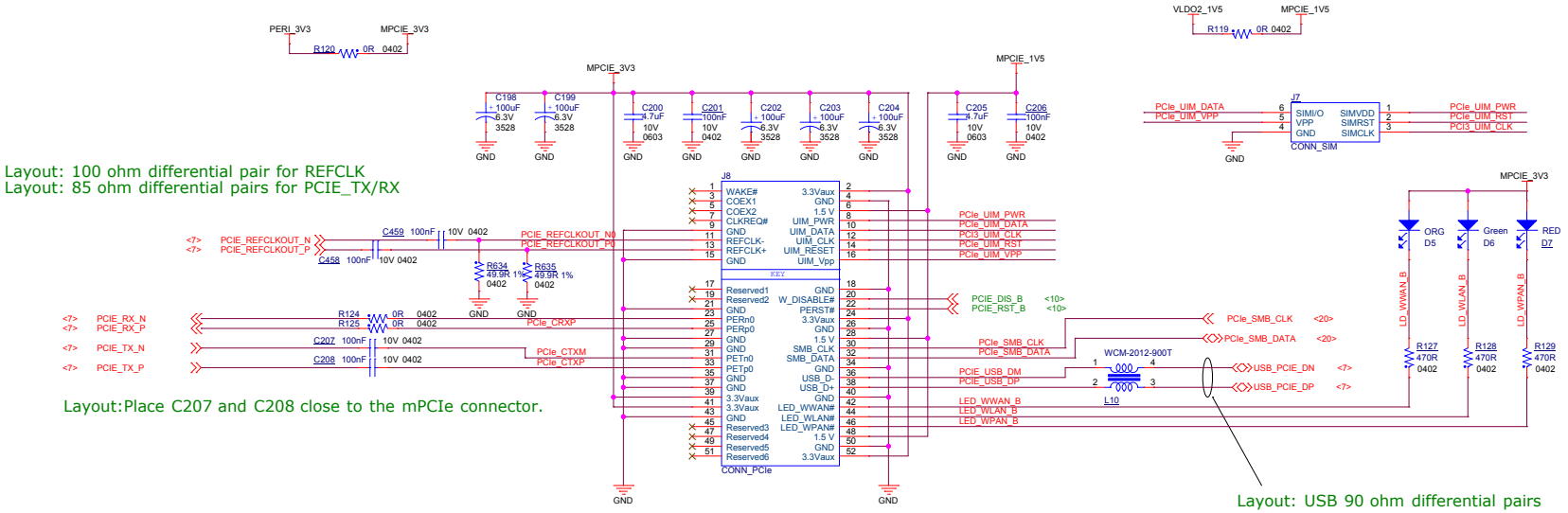
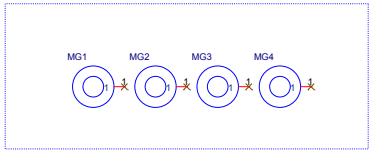
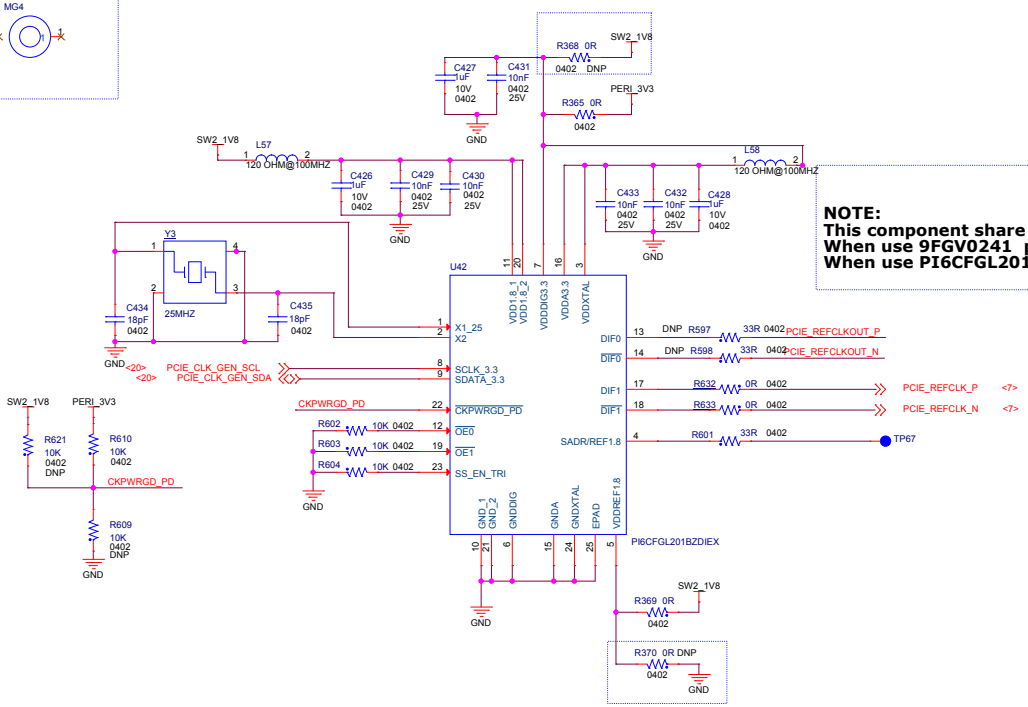
Mini-PCIE



STANDOFF



NOTE:
This design assumes a normal loading on the MPCIE_3V3 rail of up to 1A.
The MPCIE_1V5 rail is allowed a maximum of 250 mA.



NOTE:
This component share PCB package
When use 9FGV0241 populate R368 & R370, de-populate R365 & R369.
When use PI6CFGL201BZDIEX populate R365 & R369, de-populate R368 & R370 (default).

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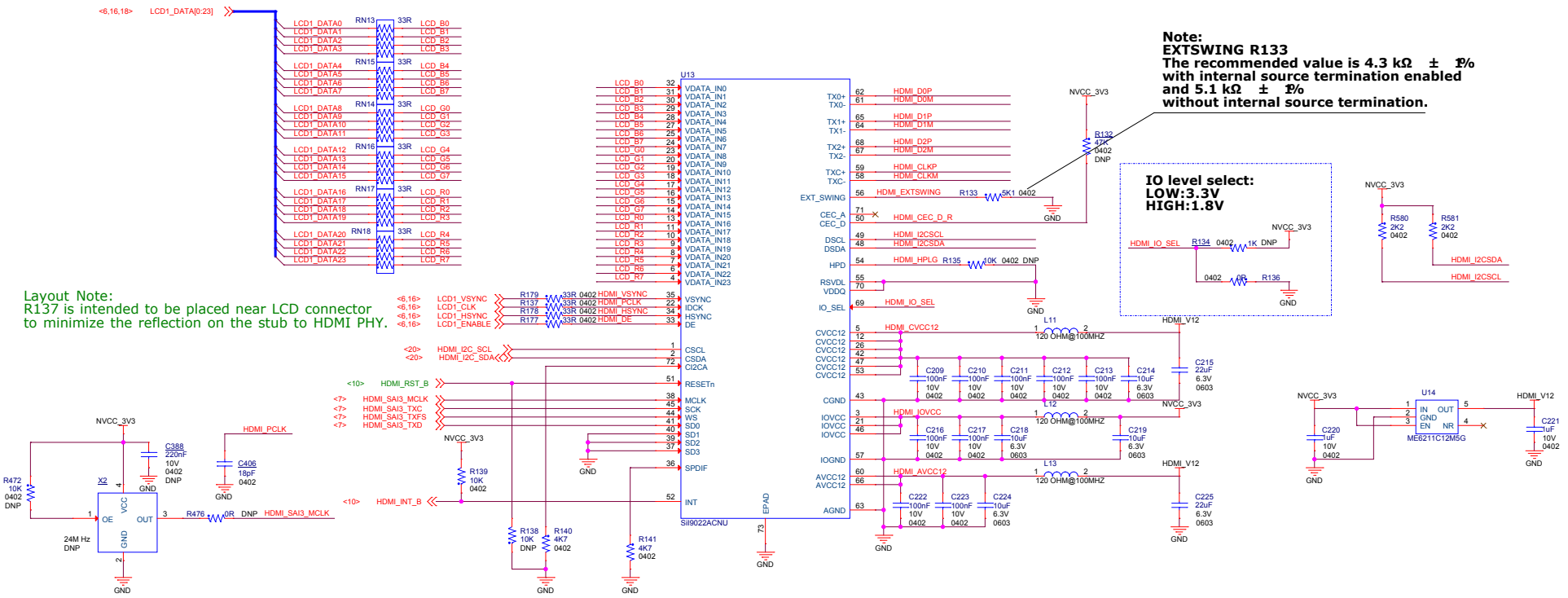
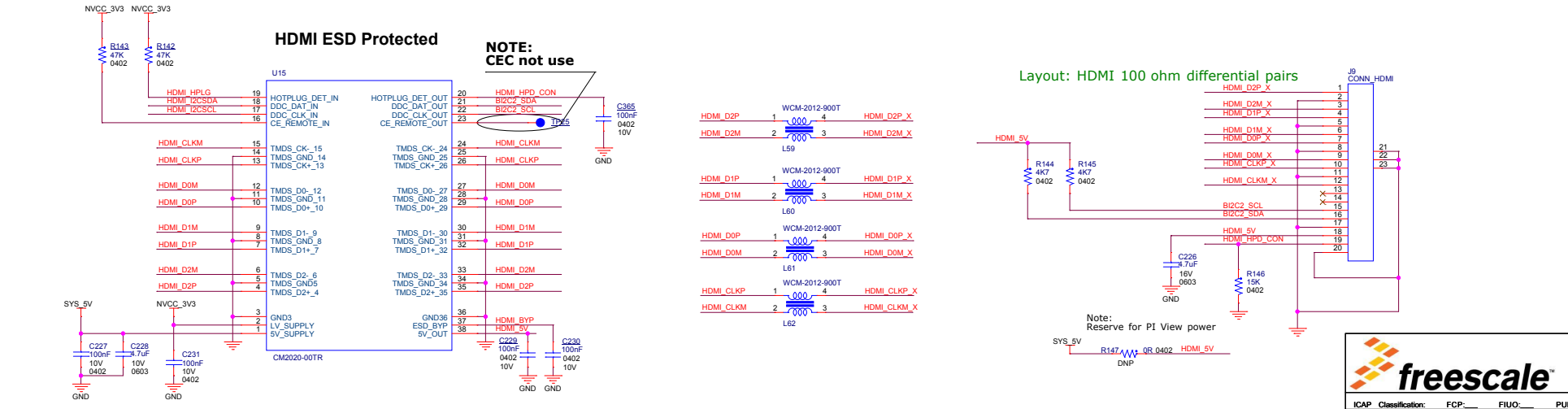
HDMI Transceiver





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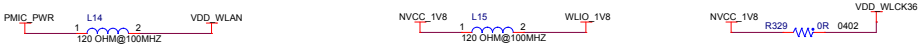
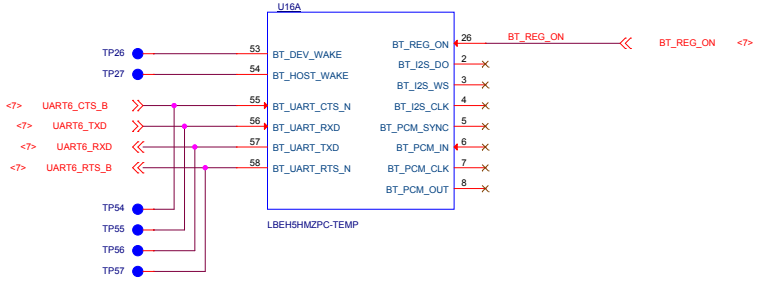
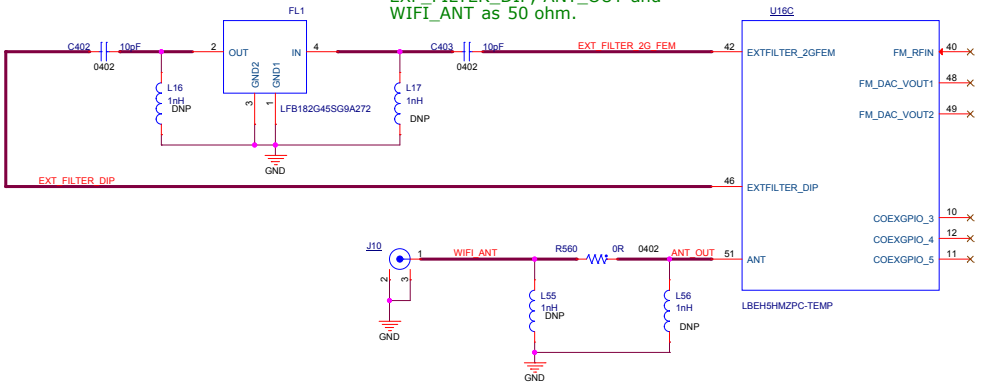
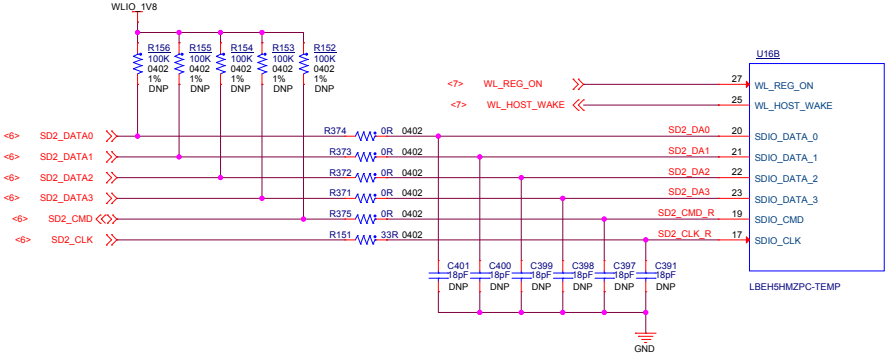
WiFi/BT



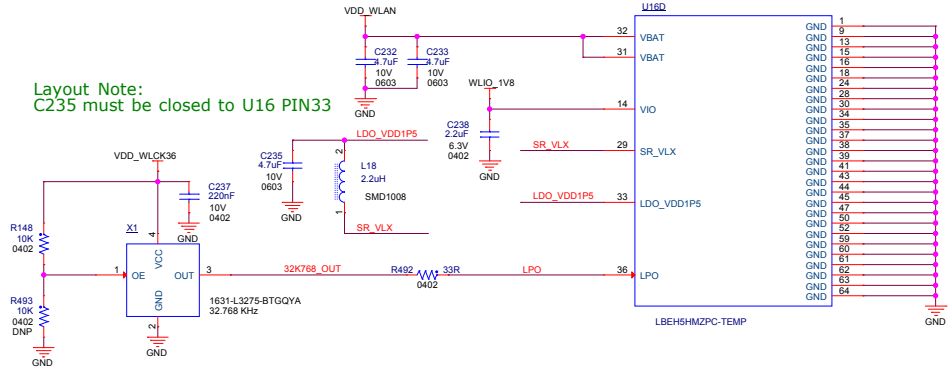


Layout: route EXT_FILTER_2G_FEM, EXP_FILTER_DIP, ANT_OUT and WIFI_ANT as 50 ohm.





Layout Note:
C235 must be closed to U16 PIN33



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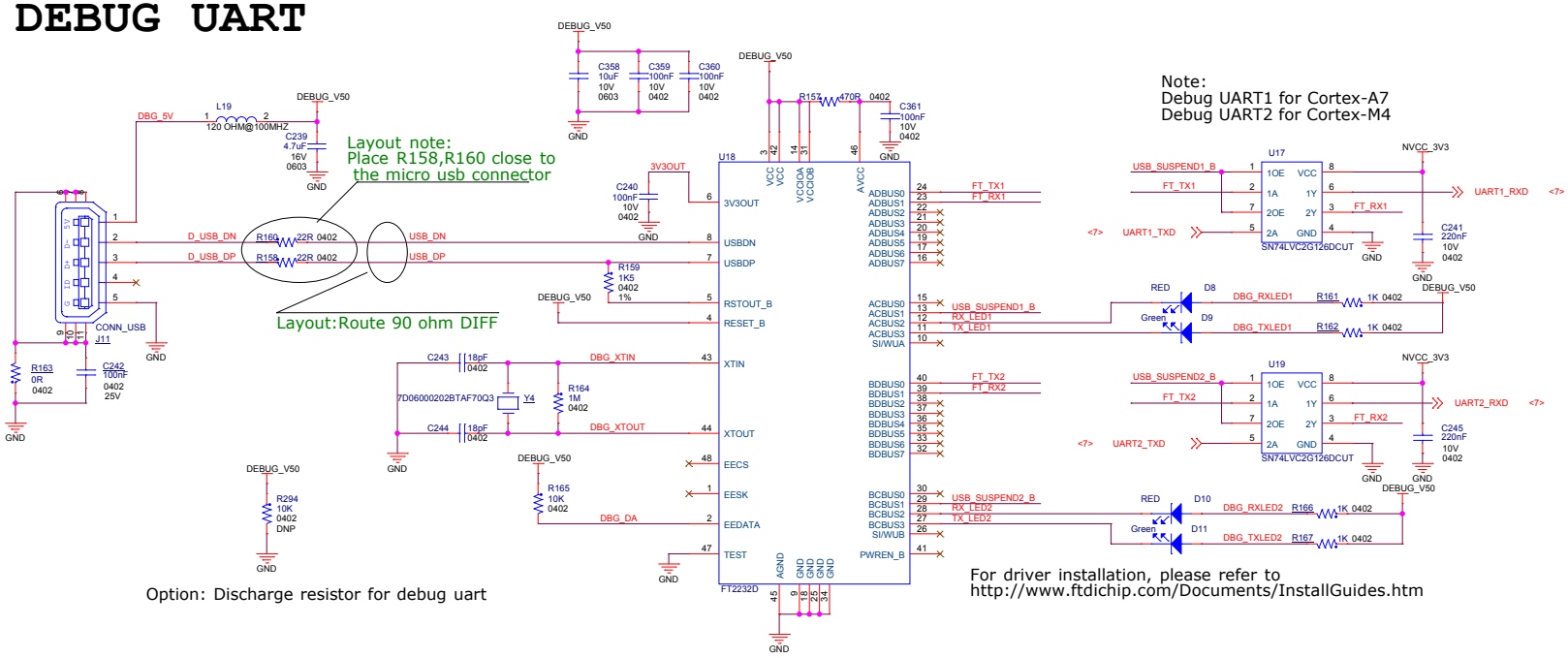
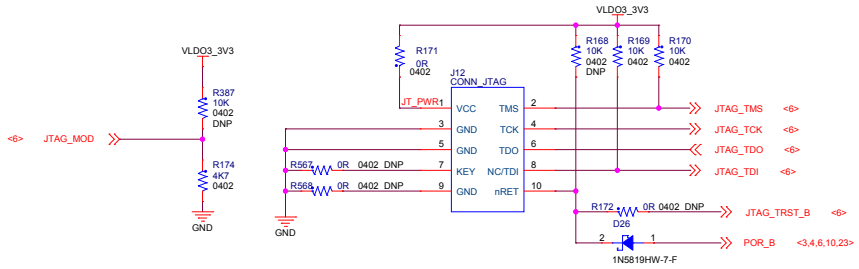
DEBUG UART



JTAG



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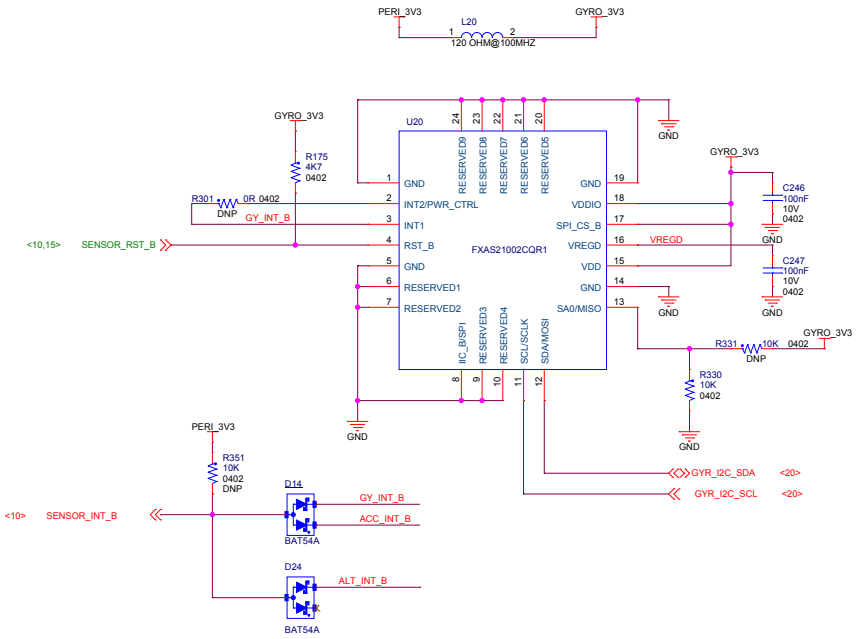
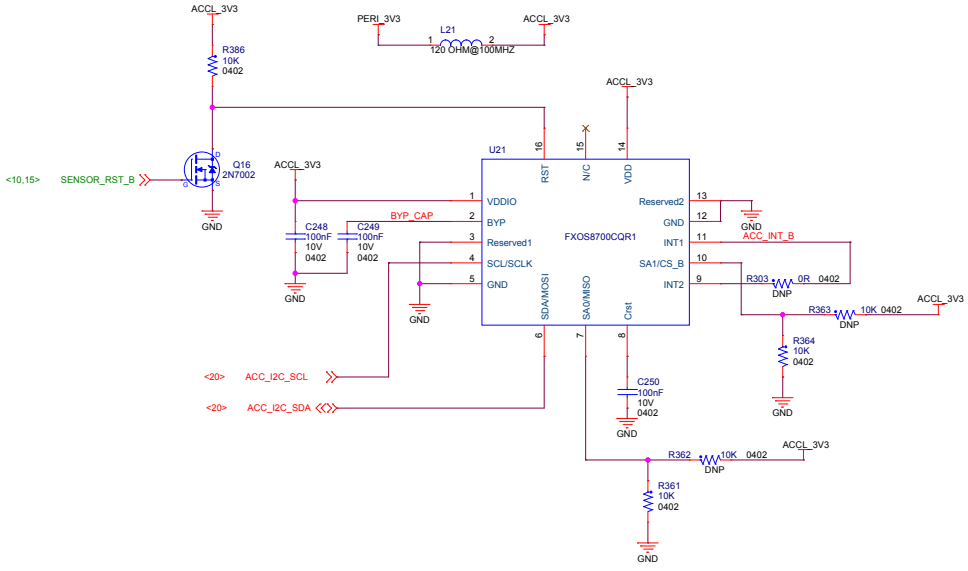
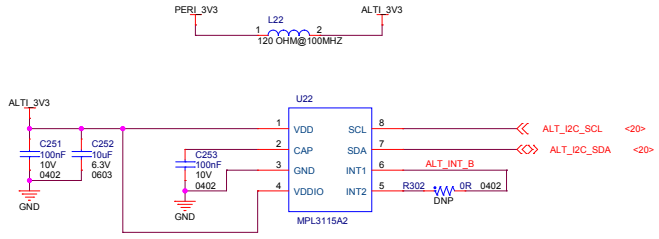
Gyroscope



Accelerometer & Magnetometer



Barometer/Altimeter



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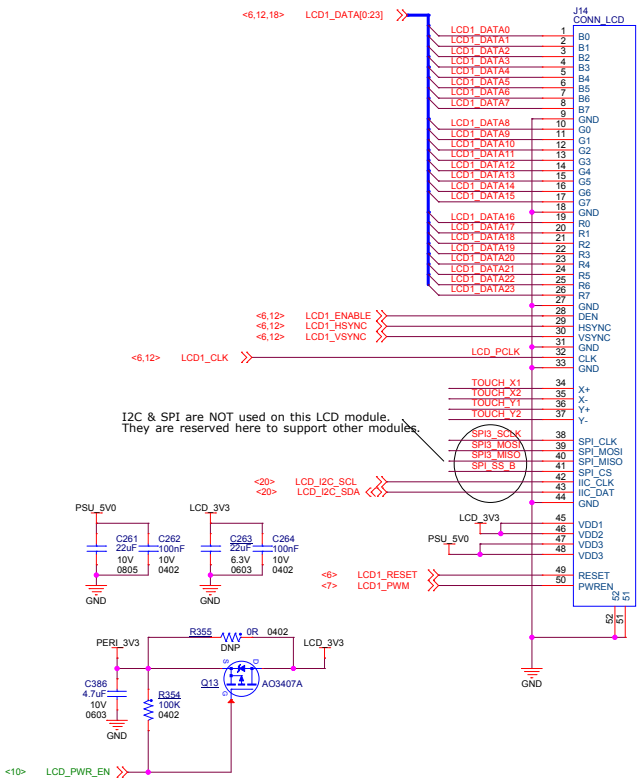
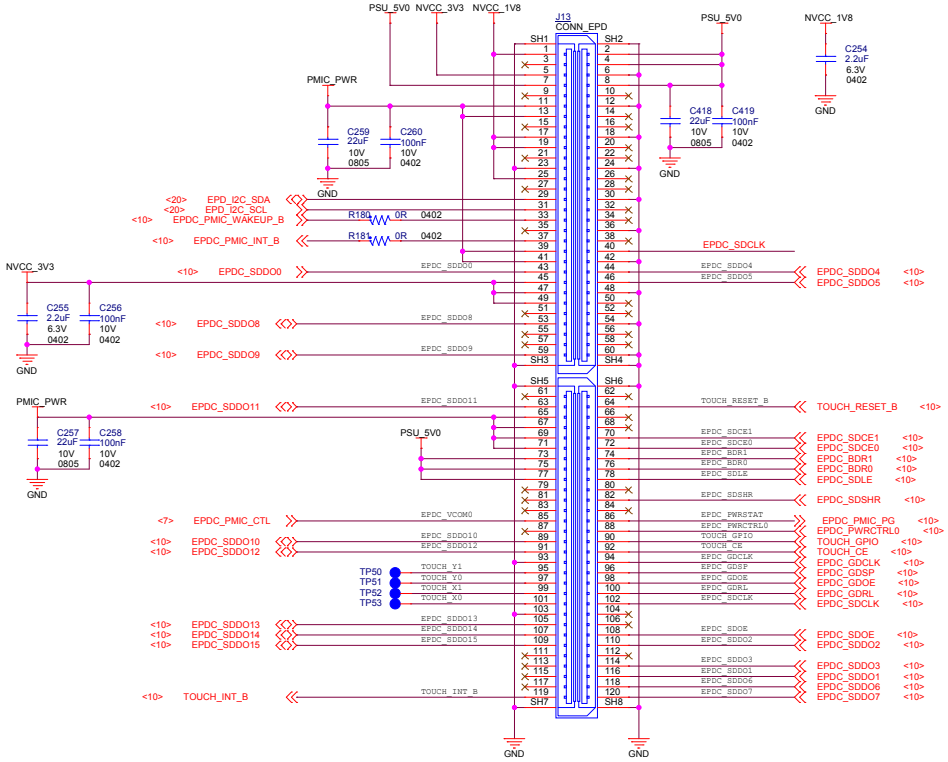
LCD

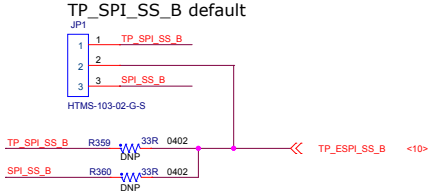
LCD8000-43T from Embest

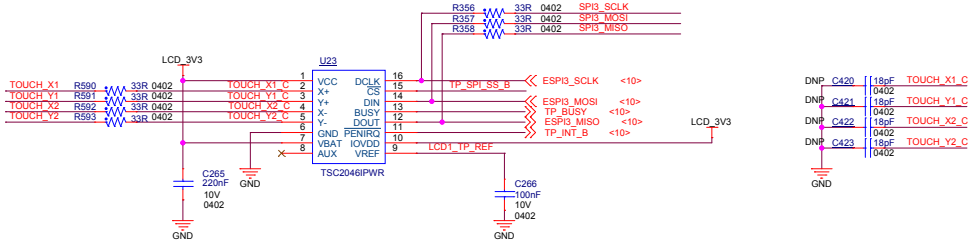


EPD



Note:
TP_SPI_SS_B default





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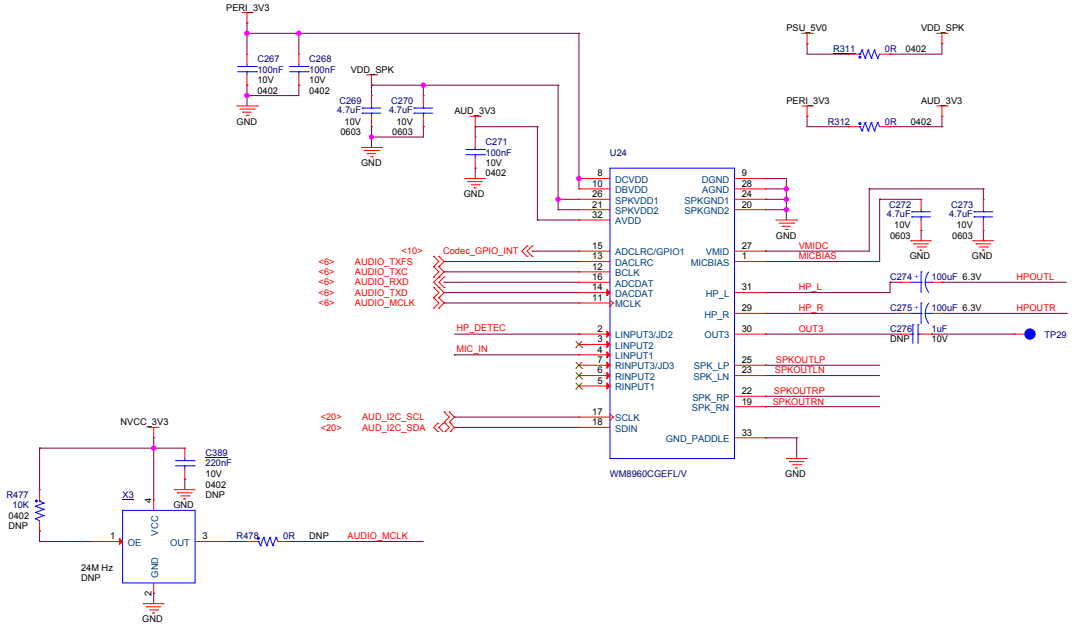
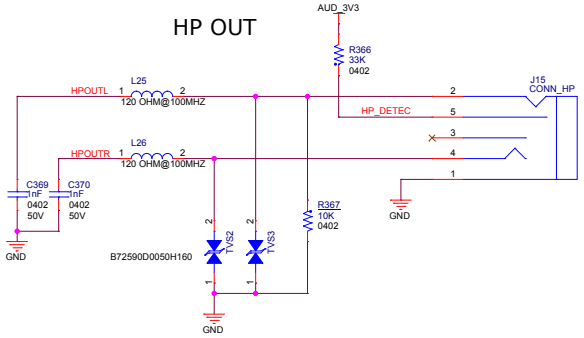
AUDIO

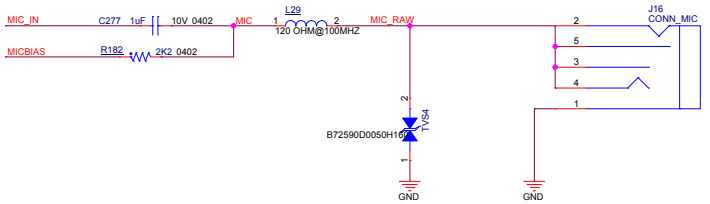


HP OUT



Speaker Out

MIC IN



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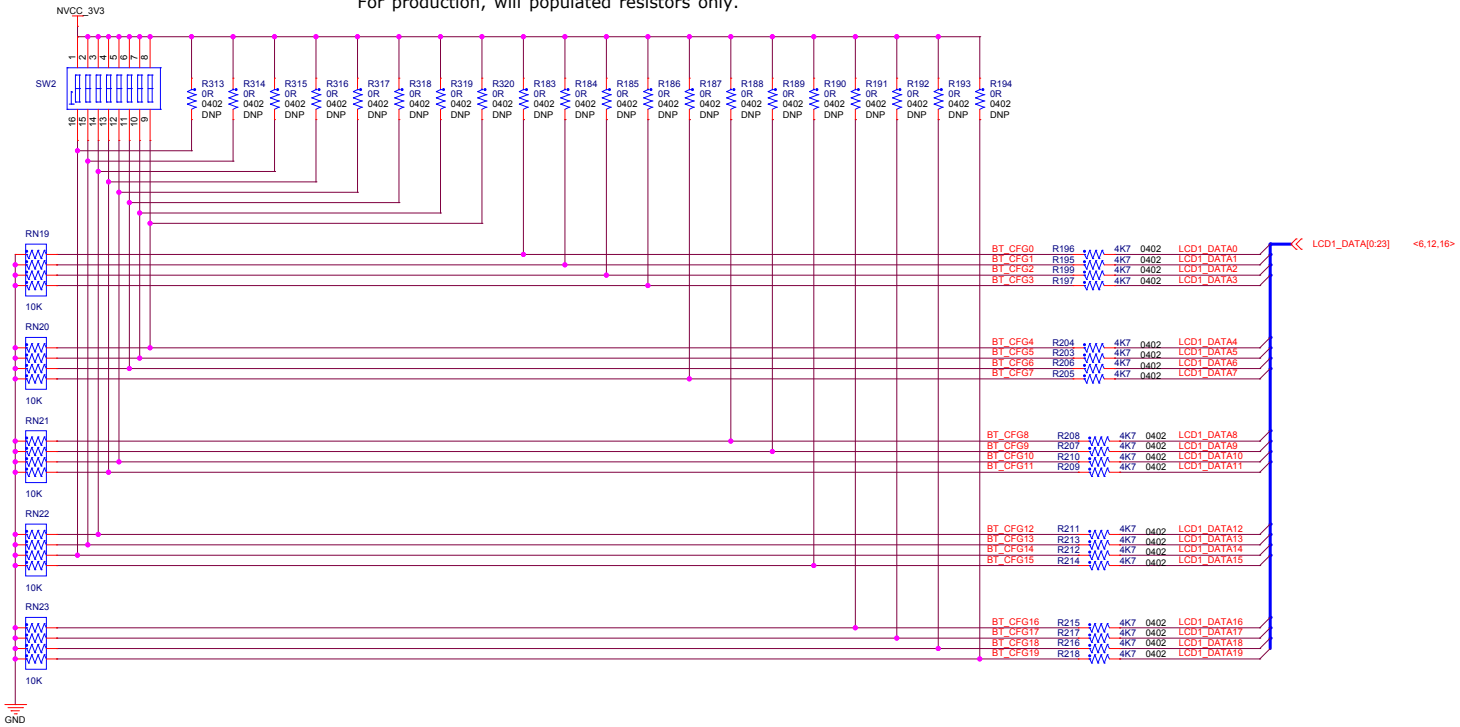
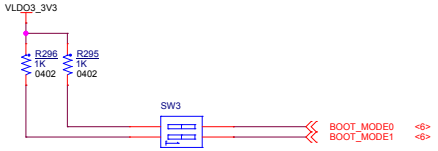
Boot Config

SW2 will be populated on pro.
For production, will populated resistors only.

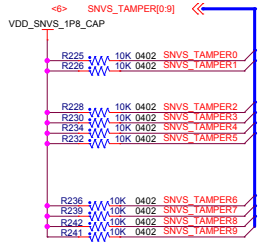


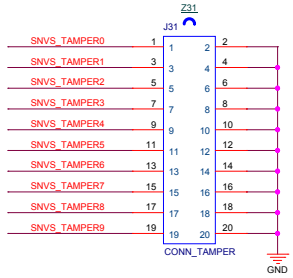
BOOT MODE

BOOT_MODE	[1]	[0]
FUSES	0	0
Serial Downloader	0	1
INTERNAL BOOT	1	0
TEST MODE	1	1



TAMPER





BOOT TABLE

SW2

1	2	3	4	5	6	7	8
BT_CFG[14]	BT_CFG[13]	BT_CFG[12]	BT_CFG[11]	BT_CFG[10]	BT_CFG[6]	BT_CFG[5]	BT_CFG[4]
001 = SD/eSD Boot			Port Select: 00 – eSDHC1 01 – eSDHC2 10 – eSDHC3		0	0	Bus Width: 0 – 1-bit 1 – 4-bit
010 = MMC/eMMC Boot					Bus Width: 000 – 1-bit 001 – 4-bit 010 – 8-bit 101 – 4-bit DDR (MMC 4.4) 110 – 8-bit DDR (MMC 4.4)		
011 = NAND Boot			Pages In Block: 00 – 128 01 – 64 10 – 32 11 – 256		BOOT_SEARCH_COUNT: 00 – 2 01 – 2 10 – 4 11 – 8		0
100 = QSPI Boot			0	0	0	0	0

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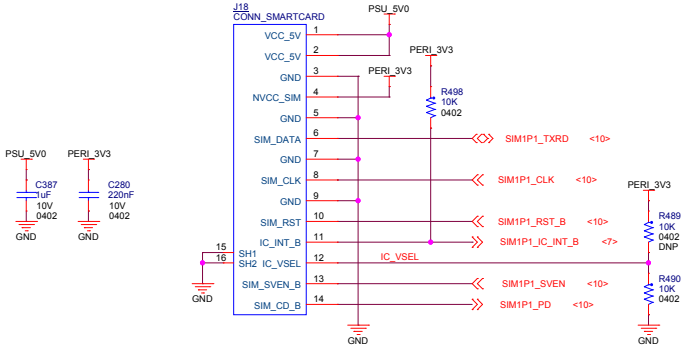
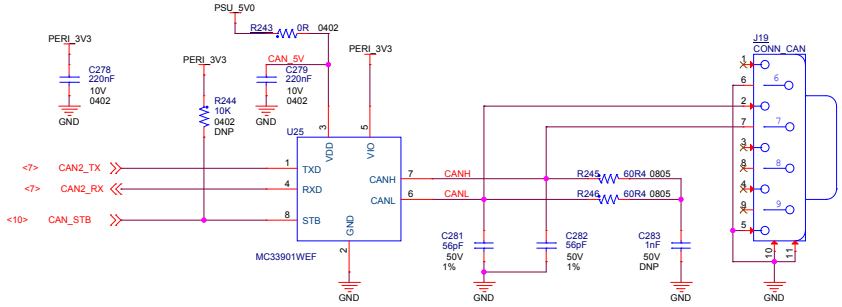
ISO7816

Connector J18 is compatible with SCH-28609_B.

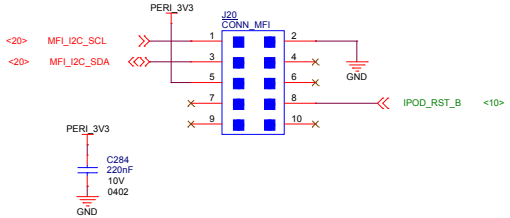


Add a note:
IC_VSEL
L: Card VCC = 3V
H: Card VCC = 1.8V

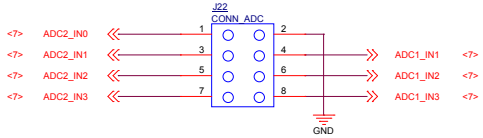
CAN



MFI



ADC



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ICAP Classification: FCP:___ FIUO:___ PUBI: X

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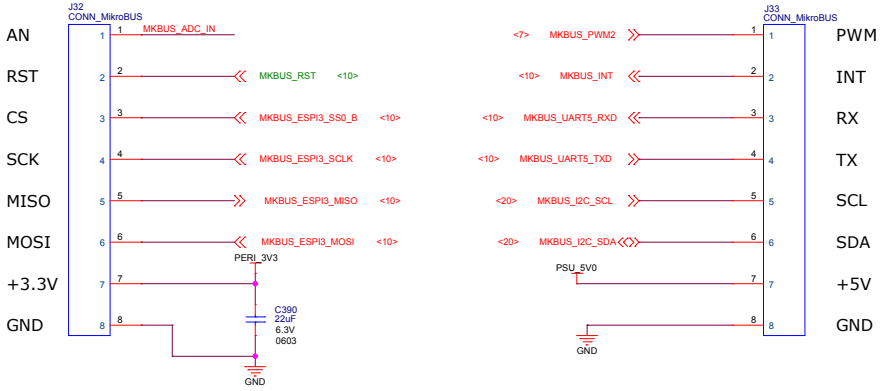
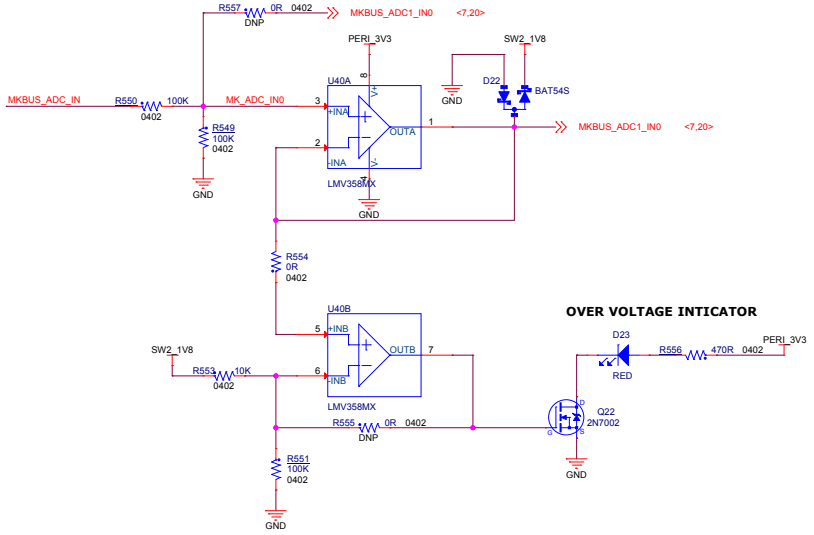
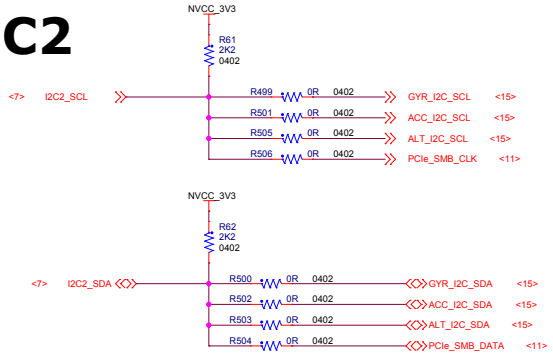
MikroBUS

http://www.mikroe.com/

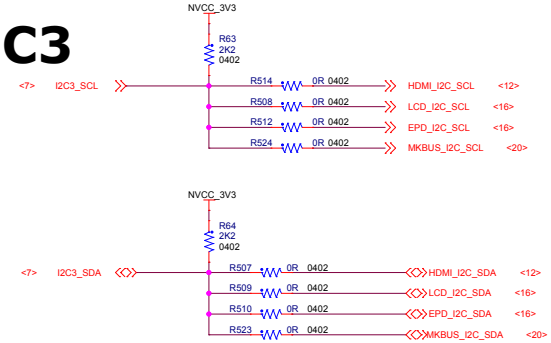




I2C2

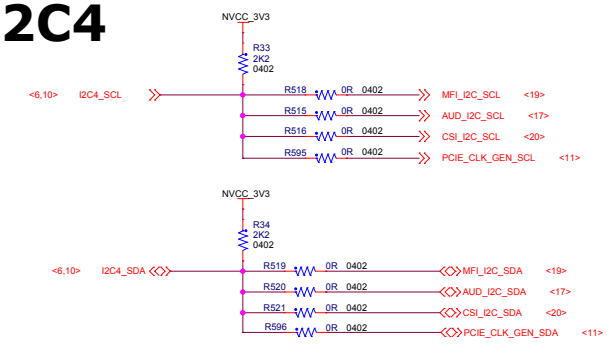


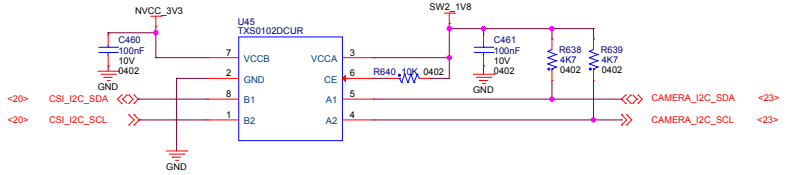
I2C3



Note: Pull-up resistor must be sized to meet the signal rise times and also the Vil spec of all the bus components. Due to board loadings this resistor was reduced. Validate your design, with the largest allowable resistor to reduce current consumption.

I2C4





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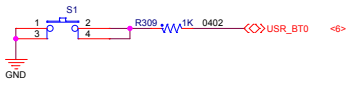
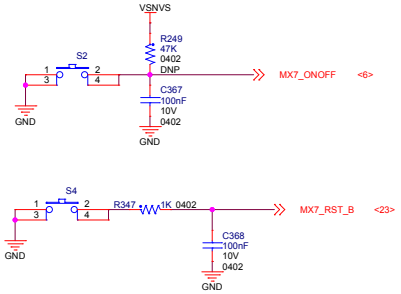
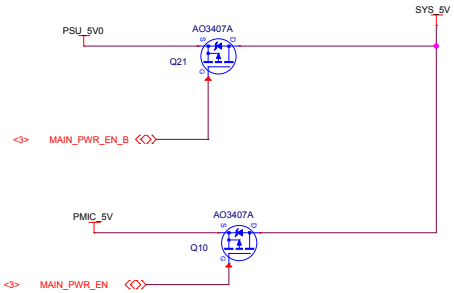
User Button



Power Botton

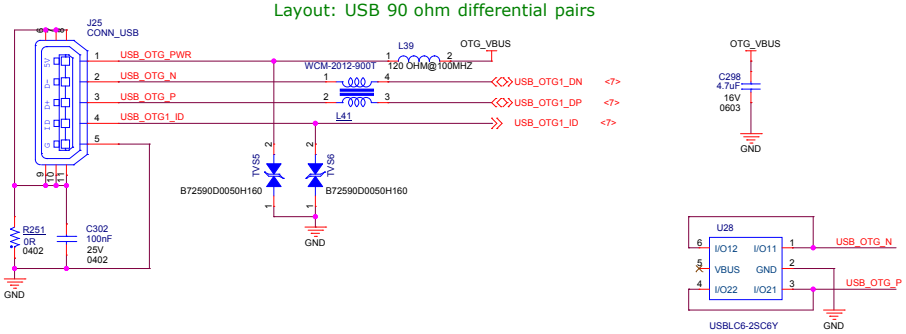


5V Power Switch



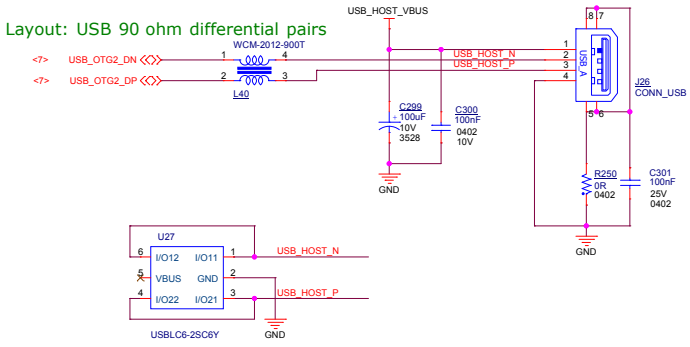
USB OTG

Layout: USB 90 ohm differential pairs



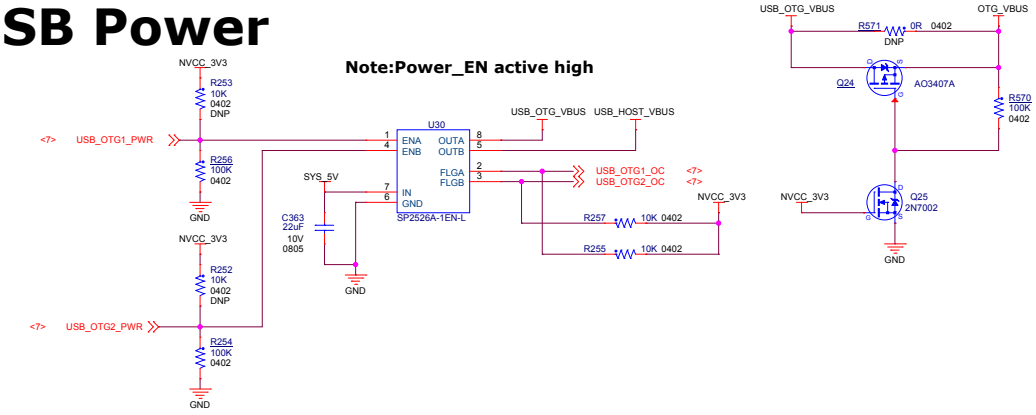
USB HOST

Layout: USB 90 ohm differential pairs



USB Power

Note:Power_EN active high



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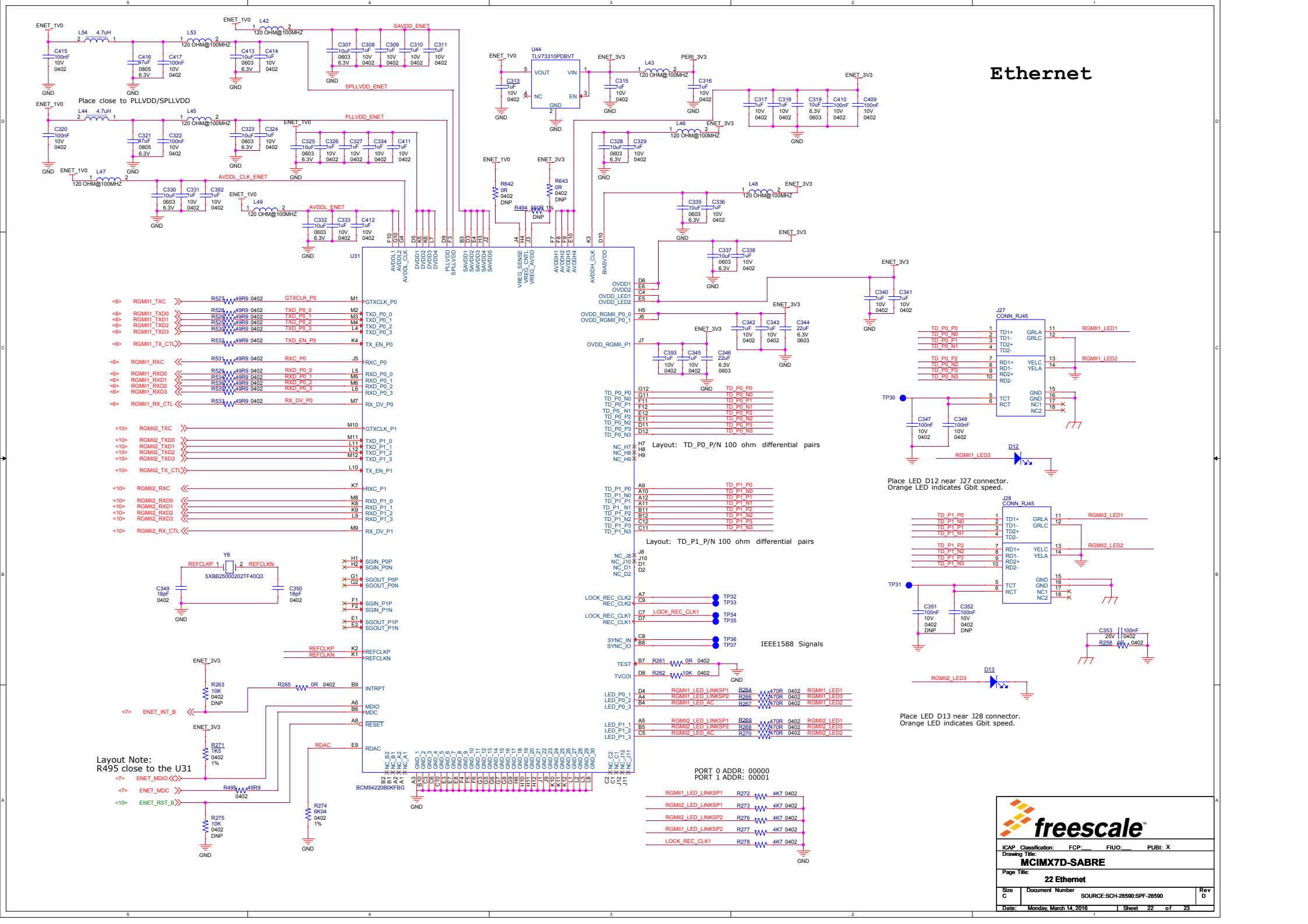
Ethernet



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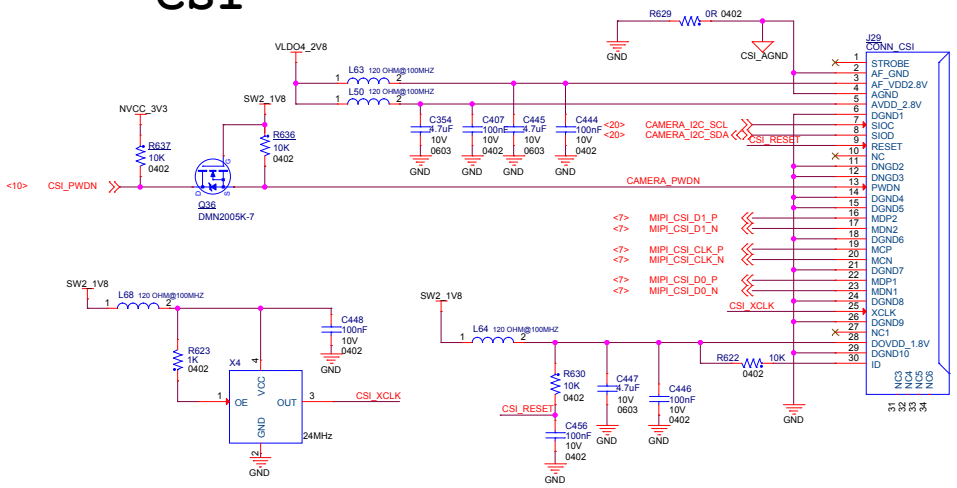
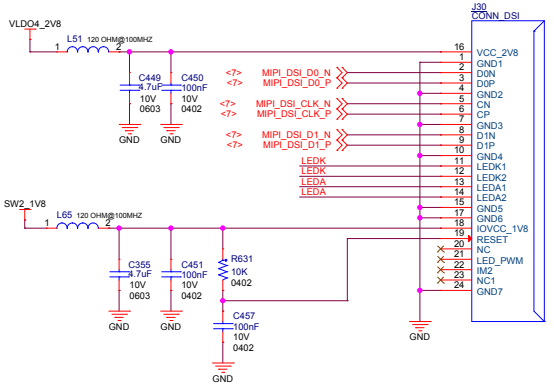
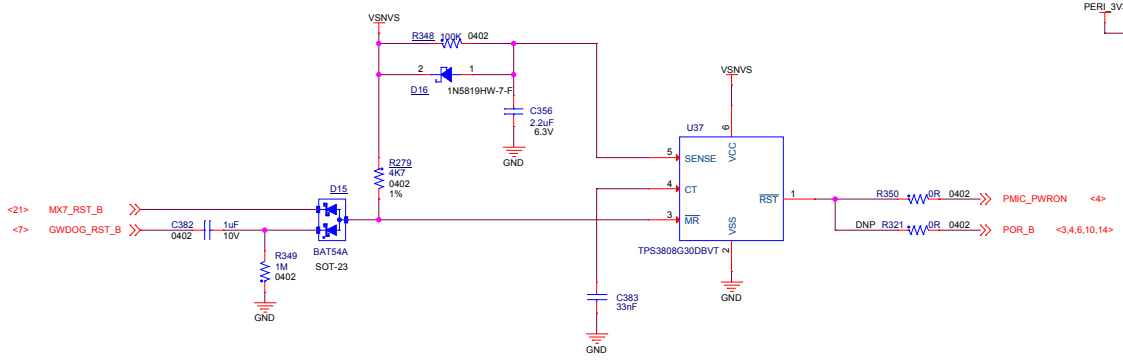
CSI



DSI

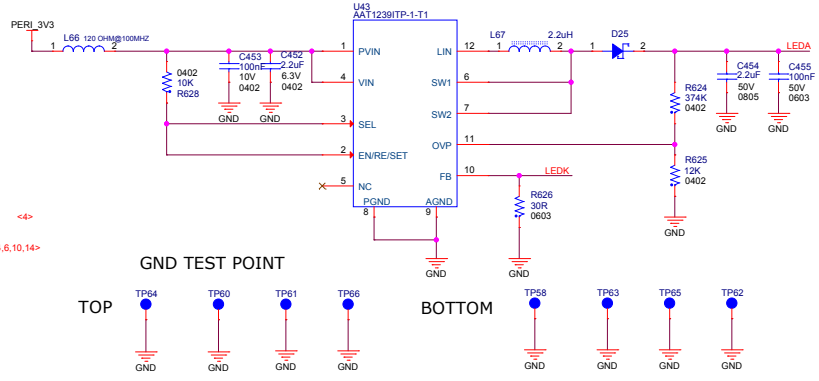


WATCH DOG



LED BKL POWER

NOTE:
Used R626=30R set the maximum led current is 20mA.



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ICAP Classification: FCP:___ FIUO:___ PUBI: X

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