# Introduction

|  |  |
| --- | --- |
| IP quick facts | |
| Supported device families | Zynq®-7000, 7 series |
| Supported user interfaces | Xilinx®: AXI4-Lite, rx\_mipi\_ppi |
| **Provided with core** | |
| Design files | VHDL |
| Simulation model | VHDL Behavioral |
| Constraints file | XDC |
| Software driver | standalone |
| **Tested design flows** | |
| Design entry | Vivado™ Design Suite 2017.4 |
| Synthesis | Vivado Synthesis 2017.4 |

This user guide describes the Digilent MIPI D-PHY Receiver Intellectual Property. This IP is compatible with D-PHY 1.0 specifications and serves as the lowest layer of the high-speed source-synchronous interface defined by MIPI Alliance. It pairs up with a MIPI CSI-2 Receiver IP over the standard PHY Protocol Interface (PPI) to receive data from an image sensor and source a video subsystem. The physical interconnect for Xilinx 7-series FPGA relies on techniques outlined in XAPP894[1].

# Features

* Single or dual lane support
* CIL-SFEN, CIL-SCNN lane implementation: unidirectional, Control and High-Speed modes
* Xilinx interfaces used: AXI4-Lite, rx\_mipi\_ppi\_if\_rtl:1.0
* Debug module

# Performance

The IP has been tested in dual-lane configuration with 1344 Mbps total data rate, resulting in 84 MHz PPI high-speed byte clock (RxByteClkHS).

# Resource Utilization

| Device | Configuration | Resource | | | | |
| --- | --- | --- | --- | --- | --- | --- |
| LUT | FF | BRAM | URAM | DSP |
| xc7z020clg400-1 | AXI-Lite Interface | 297 | 312 | 0 | 0 | 0 |

# Overview



Figure 1. DVI to VGA converter block diagram.

The IP is built from multiple blocks: input buffers, clock buffers, de-serializer, control logic and optional debug modules.

# Port Descriptions

| Signal Name | Interface | Signal Type | Init State | Description |
| --- | --- | --- | --- | --- |
| RefClk | - | I | N/A | 200 MHz reference clock. |
| aRst(\_n) | - | I | N/A | Asynchronous reset of configurable polarity. Assert, if RefClk is not within spec. |
| rDlyCtrlLockedIn | - | I | N/A | Available when Shared Logic is not included in the IP. It is expected to have a single master instance of D-PHY IP in the design with Shared Logic included. The port rDlyCtrlLockedOut from the master block should drive all the rDlyCtrlLockedIn ports of the slave instances (see below). |
| rDlyCtrlLockedOut | - | O | 0 | Available when Shared Logic is included in the IP. An IDELAYCTRL block with proper reset circuitry will be instantiated, which will manage all the IDELAY components of all the D-PHY instances in the design. The port rDlyCtrlLockedOut from the master block should drive all the rDlyCtrlLockedIn ports of the slave instances (see above). |

# Designing with the core

The IP expects to be connected directly to top-level ports, since input buffers are instantiated internally. Since the D-PHY I/O standard is not supported directly by FPGA pins, it implements the techniques described in [1] that separate the D-PHY lane into a differential high-speed bus (LVDS\_25) and two low-power control signals (HSUL\_12). It was verified as working with either passive or active termination. This implementation allows 3.3V-supplied HR banks to interface with D-PHY transmitters using external on-board terminations and internal voltage reference.

## Constraints

See an example below on how to constrain the low-power (LP) and high-speed (HS) input pins. Banks hosting HSUL\_12 pins need a 0.6V voltage reference, either internal or external. A primary clock with a frequency corresponding to the maximum expected data rate should be created on the clock input port.

set\_property INTERNAL\_VREF 0.6 [get\_iobanks 35]

set\_property -dict {PACKAGE\_PIN J19 IOSTANDARD HSUL\_12} [get\_ports dphy\_clk\_lp\_n]

set\_property -dict {PACKAGE\_PIN H20 IOSTANDARD HSUL\_12} [get\_ports dphy\_clk\_lp\_p]

set\_property -dict {PACKAGE\_PIN M18 IOSTANDARD HSUL\_12} [get\_ports {dphy\_data\_lp\_n[0]}]

set\_property -dict {PACKAGE\_PIN L19 IOSTANDARD HSUL\_12} [get\_ports {dphy\_data\_lp\_p[0]}]

set\_property -dict {PACKAGE\_PIN L20 IOSTANDARD HSUL\_12} [get\_ports {dphy\_data\_lp\_n[1]}]

set\_property -dict {PACKAGE\_PIN J20 IOSTANDARD HSUL\_12} [get\_ports {dphy\_data\_lp\_p[1]}]

set\_property -dict {PACKAGE\_PIN H18 IOSTANDARD LVDS\_25} [get\_ports dphy\_hs\_clock\_clk\_n]

set\_property -dict {PACKAGE\_PIN J18 IOSTANDARD LVDS\_25} [get\_ports dphy\_hs\_clock\_clk\_p]

# 672Mbps/lane = 336 MHz HS\_Clk

create\_clock -period 2.976 -name dphy\_hs\_clock\_p -waveform {0.000 1.488} [get\_ports dphy\_hs\_clock\_clk\_p]

set\_property -dict {PACKAGE\_PIN M20 IOSTANDARD LVDS\_25} [get\_ports {dphy\_data\_hs\_n[0]}]

set\_property -dict {PACKAGE\_PIN M19 IOSTANDARD LVDS\_25} [get\_ports {dphy\_data\_hs\_p[0]}]

set\_property -dict {PACKAGE\_PIN L17 IOSTANDARD LVDS\_25} [get\_ports {dphy\_data\_hs\_n[1]}]

set\_property -dict {PACKAGE\_PIN L16 IOSTANDARD LVDS\_25} [get\_ports {dphy\_data\_hs\_p[1]}]

## Customization

# Debugging

# References

1. Xilinx Inc., *XAPP894: D-PHY Solutions*, v1.0, August 25, 2014.