# Introduction

|  |  |
| --- | --- |
| IP quick facts | |
| Supported device families | Zynq®-7000, 7 series |
| Supported user interfaces | Xilinx®: AXI4-Lite, AXI-Stream, rx\_mipi\_ppi |
| **Provided with core** | |
| Design files | VHDL |
| Simulation model | VHDL Behavioral |
| Constraints file | XDC |
| Software driver | standalone |
| **Tested design flows** | |
| Design entry | Vivado™ Design Suite 2017.4 |
| Synthesis | Vivado Synthesis 2017.4 |

This user guide describes the Digilent MIPI CSI-2 Receiver Intellectual Property. This IP is compatible with CSI-2 1.0 specifications and supports decoding selected pixel formats and packing data into an AXI-Stream. It pairs up with a MIPI D-PHY Receiver IP over the standard PHY Protocol Interface (PPI) to source a video subsystem.

# Features

* Single or dual lane support
* RAW10 support
* Four pixels per beat AXI-Stream output for high bandwidth applications
* Xilinx interfaces used: AXI4-Lite, AXI-Stream, rx\_mipi\_ppi\_if\_rtl:1.0

# Performance

The IP has been tested in dual-lane configuration with an 84 MHz PPI high-speed byte clock (RxByteClkHS) and 150 MHz AXI-Stream clock (video\_aclk).

# Resource Utilization

| Device | Configuration | Resource | | | | |
| --- | --- | --- | --- | --- | --- | --- |
| LUT | FF | BRAM | URAM | DSP |
| xc7z020clg400-1 | AXI-Lite Interface | 430 | 693 | 2.5 | 0 | 0 |

# Overview



Figure 1. DVI to VGA converter block diagram.

The IP is built from multiple blocks: lane merger, link-level protocol/video formatter, control logic and optional debug modules.

# Port Descriptions

# Designing with the core

## Constraints

## Customization

# Debugging

# References