
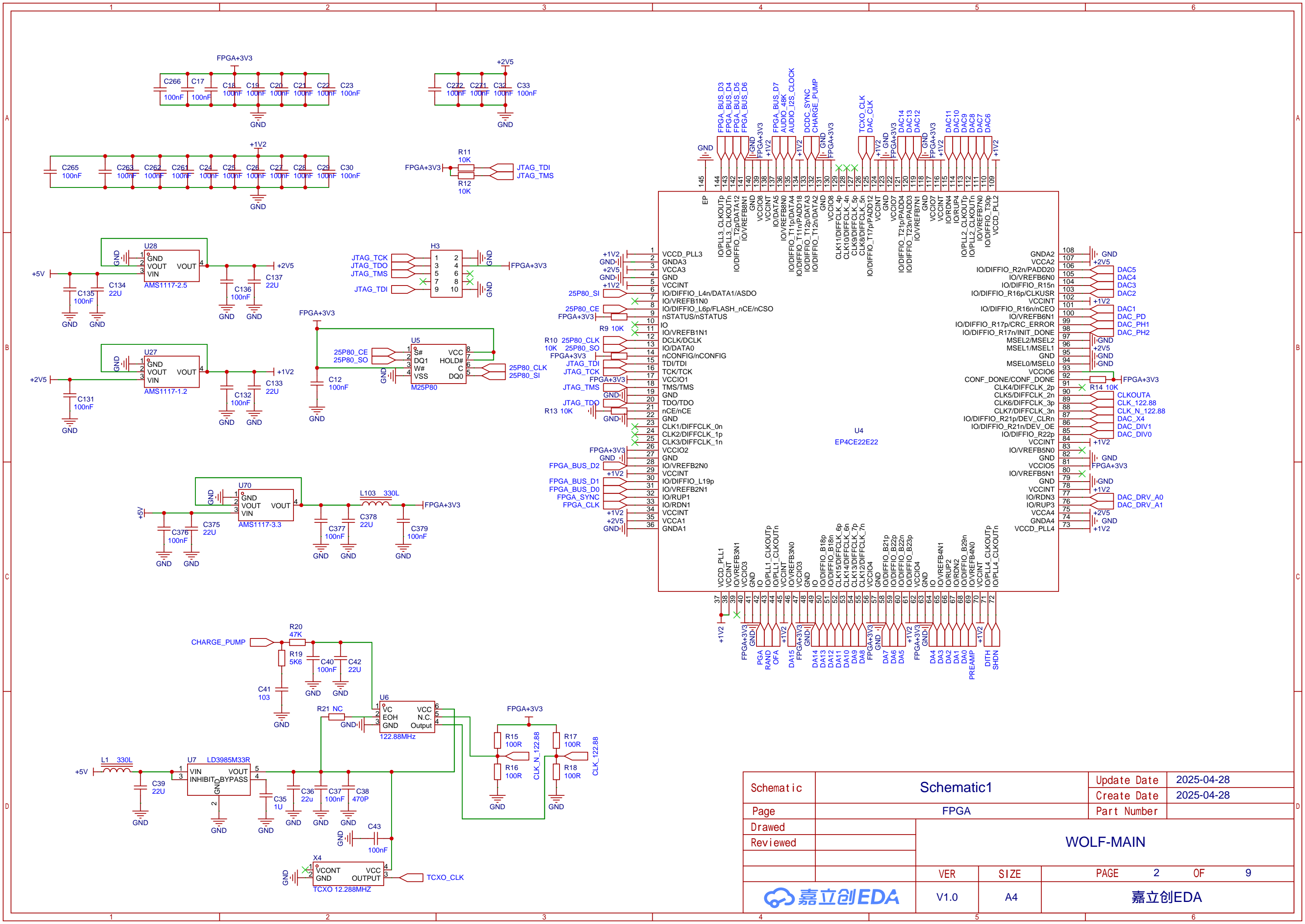

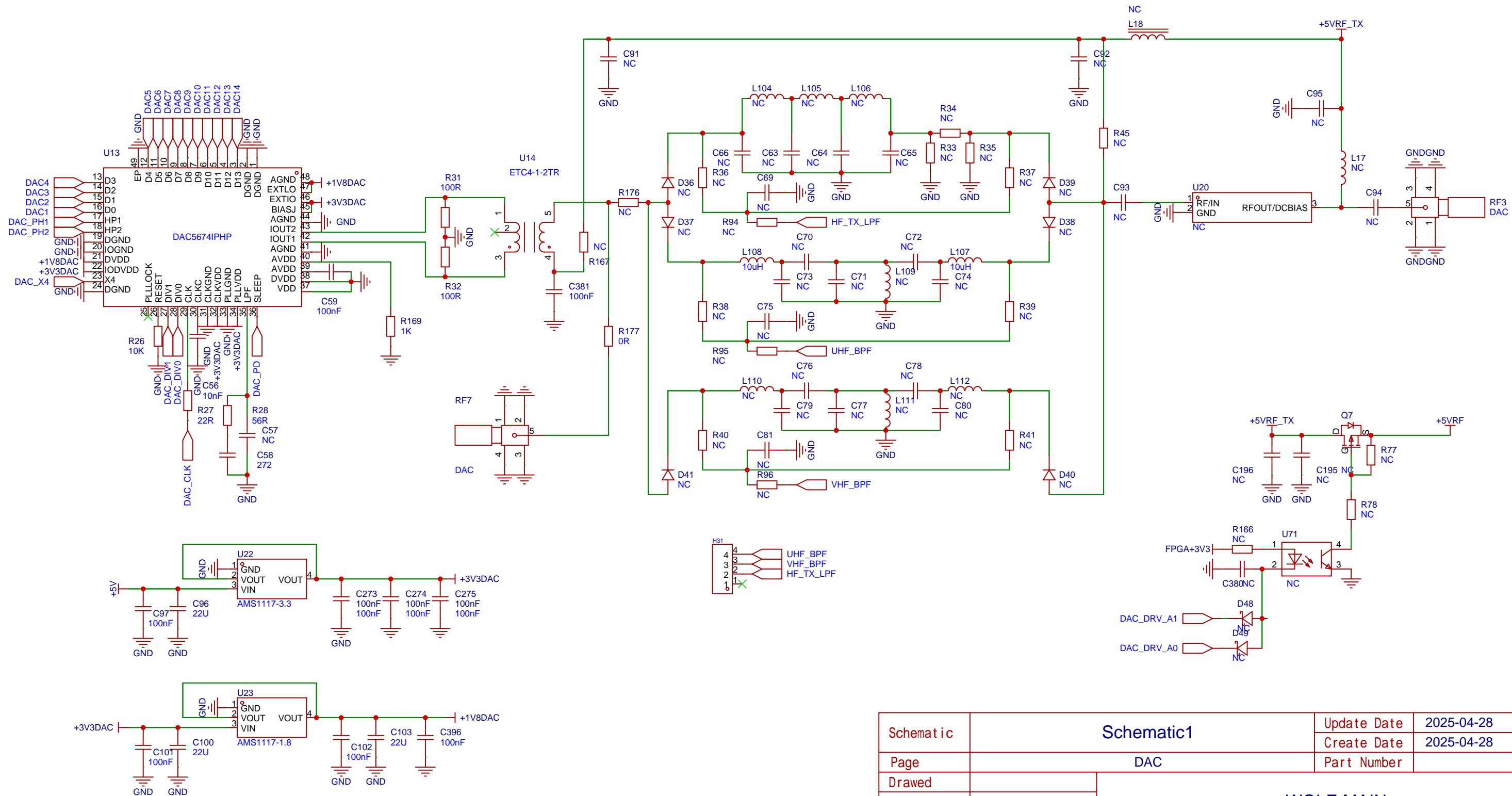


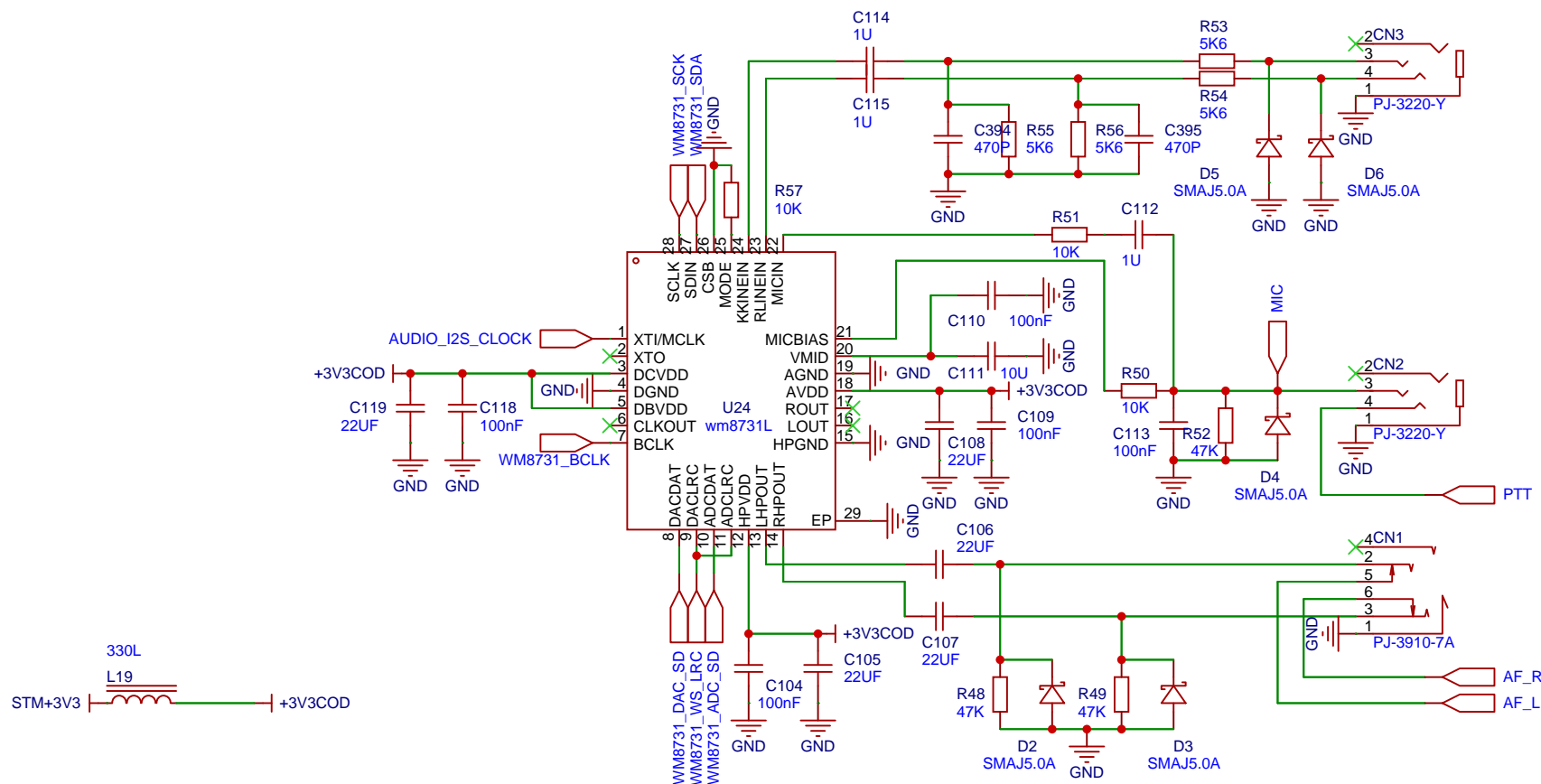
Schematic	Schematic1			Update Date	2025-04-28	
				Create Date	2025-04-28	
Page	STM32			Part Number		
Drawn		WOLF-MAIN				
Reviewed						
		VER	SIZE	PAGE	1	OF 9
		V1.0	A4	嘉立创EDA		



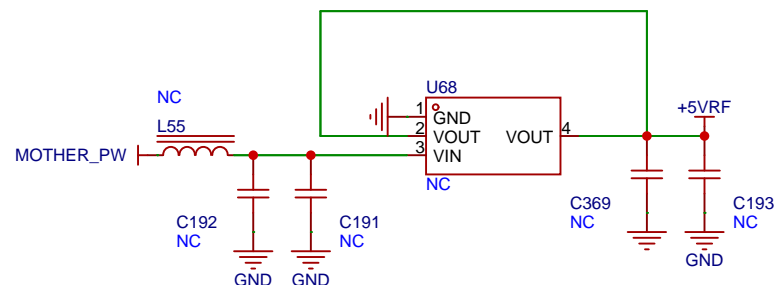
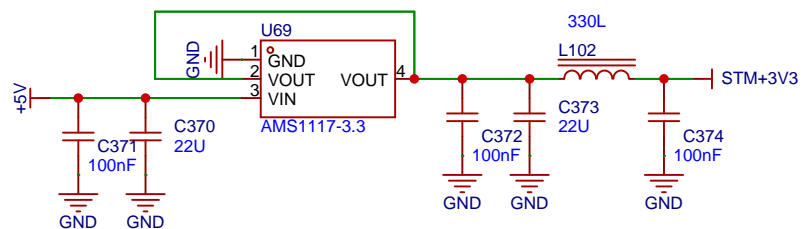
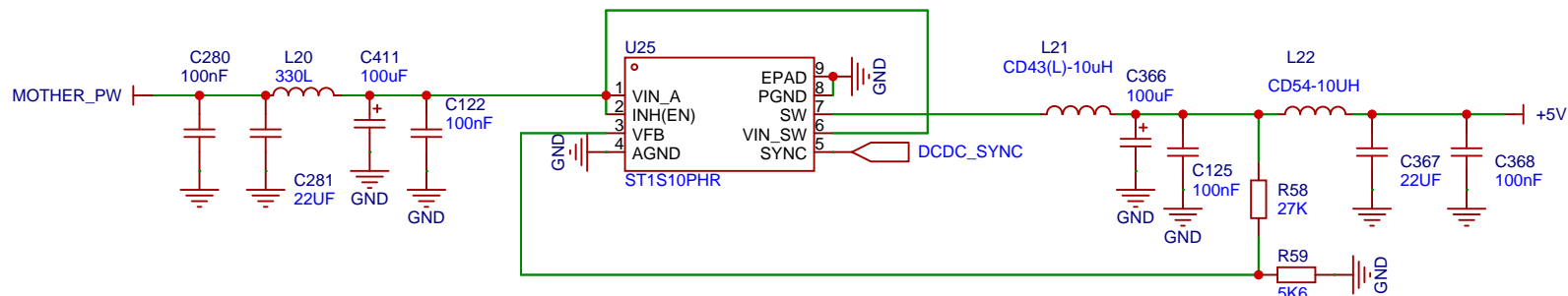
Schematic	Schematic1			Update Date	2025-04-28	
				Create Date	2025-04-28	
Page	FPGA			Part Number		
Drawn		WOLF-MAIN				
Reviewed						
		VER	SIZE	PAGE	2	OF 9
		V1.0	A4	嘉立创EDA		



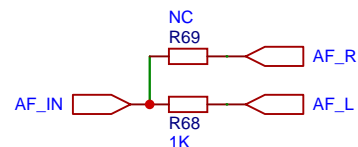
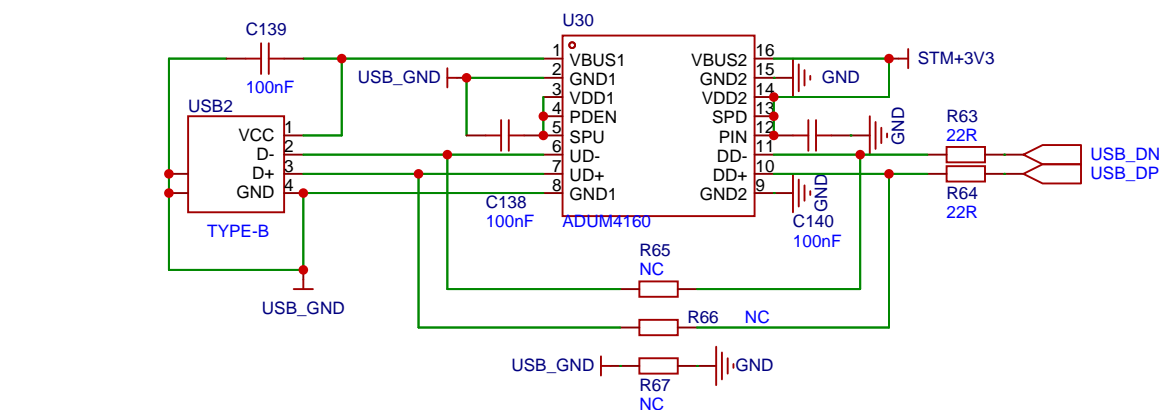
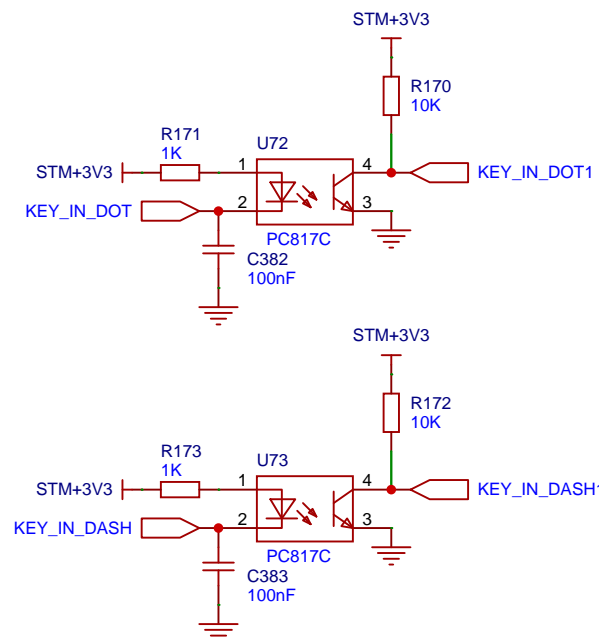
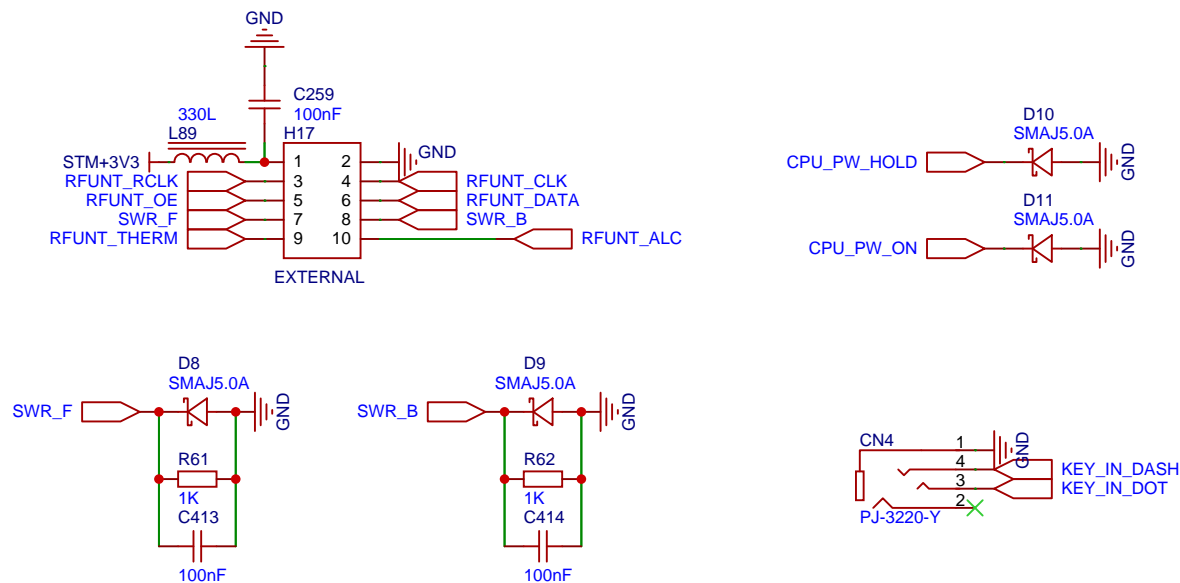
Schematic	Schematic1			Update Date	2025-04-28
				Create Date	2025-04-28
Page	DAC			Part Number	
Drawn	WOLF-MAIN				
Reviewed					
		VER	SIZE	PAGE	4 OF 9
嘉立创EDA		V1.0	A4	嘉立创EDA	




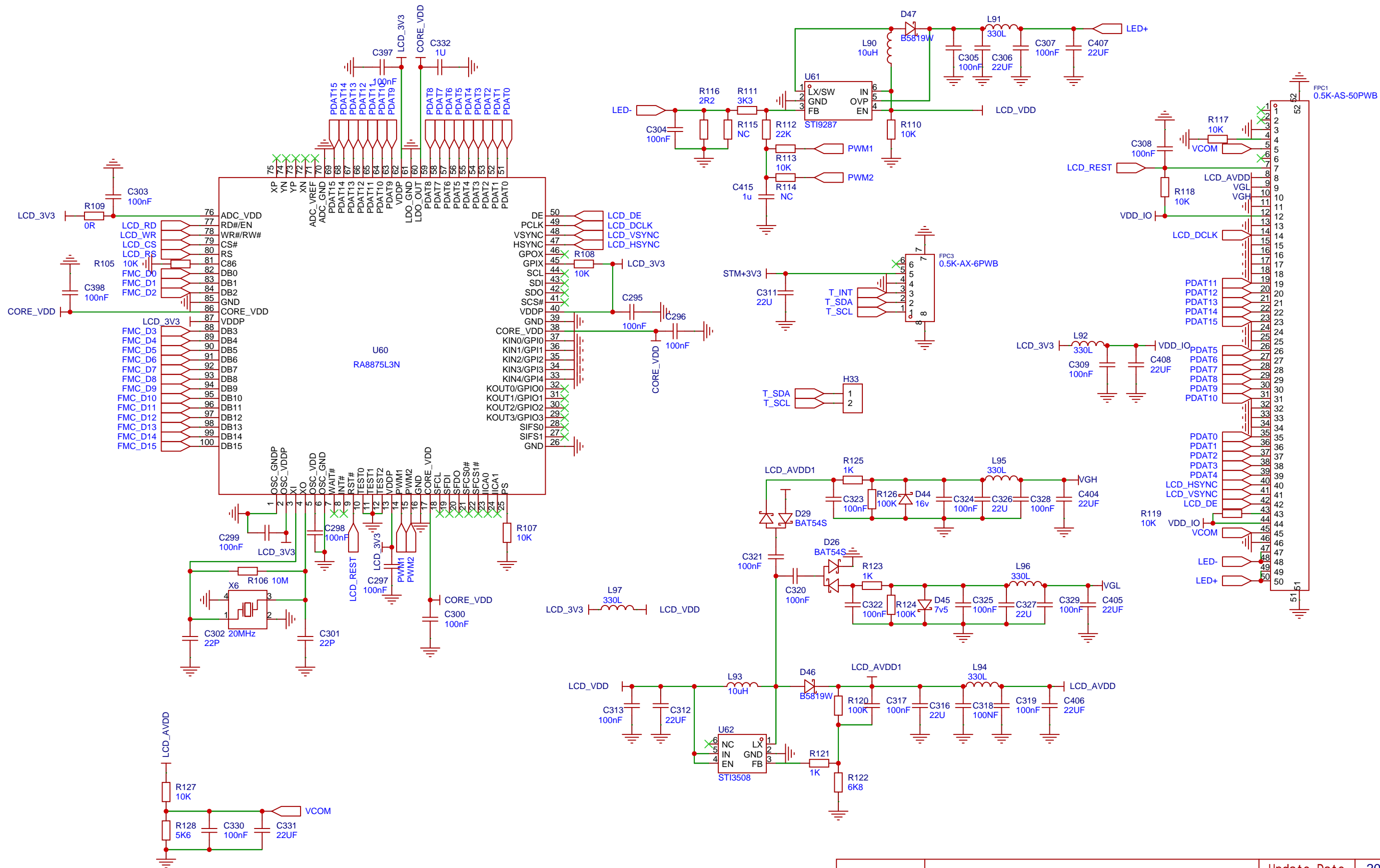
Schematic	Schematic1		Update Date	2025-04-28
			Create Date	2025-04-28
Page	CODEC		Part Number	
Drawn	WOLF-MAIN			
Reviewed				
	VER	SIZE	PAGE	5 OF 9
嘉立创EDA		V1.0	A4	嘉立创EDA




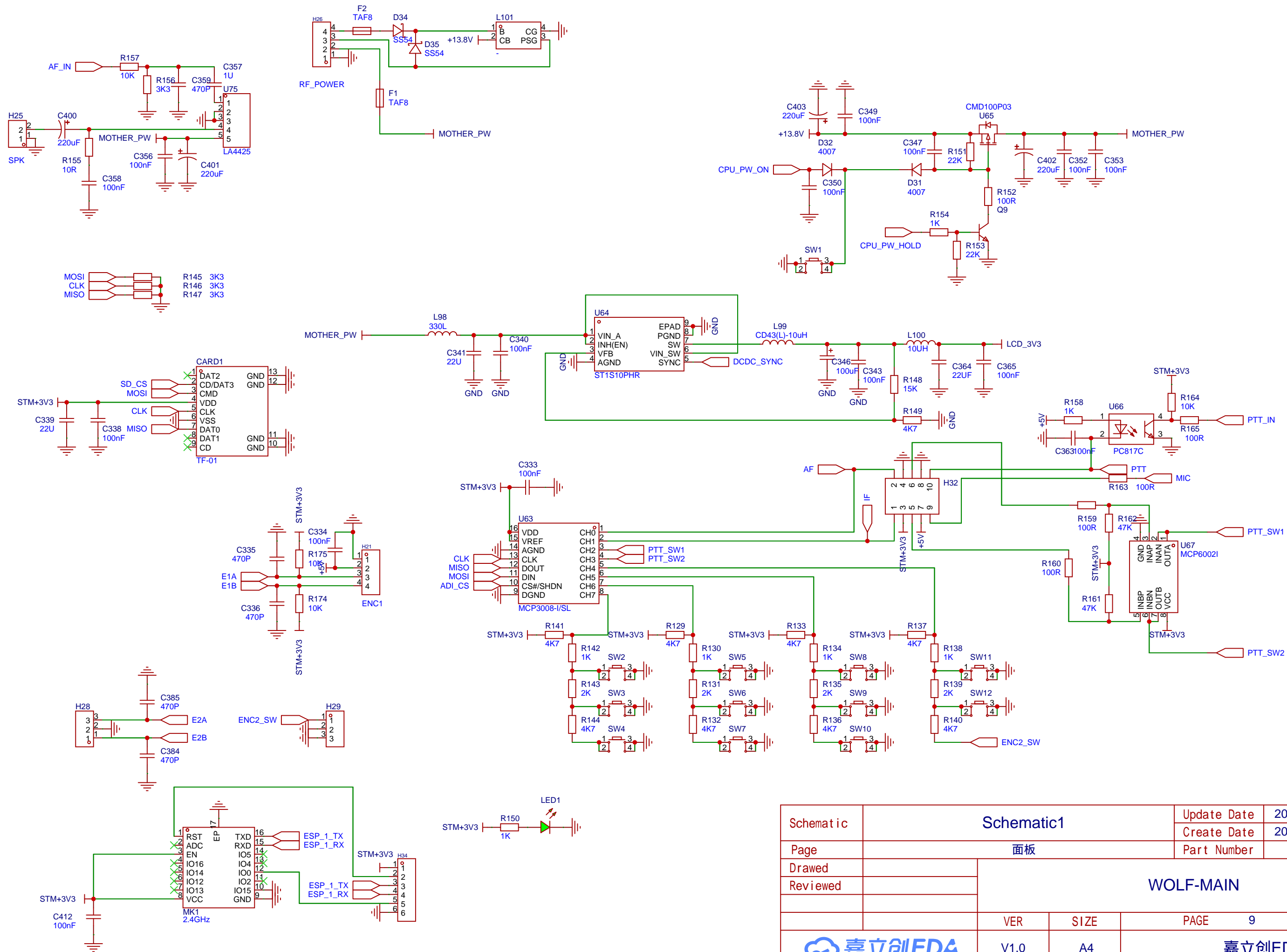
Schematic	Schematic1			Update Date	2025-04-28
Page	POWER			Create Date	2025-04-28
Drawn		WOLF-MAIN			
Reviewed					
		VER	SIZE	PAGE	6 OF 9
		V1.0	A4	嘉立创EDA	



Schematic	Schematic1			Update Date	2025-04-28
				Create Date	2025-04-28
Page	CONNECTORS			Part Number	
Drawed		WOLF-MAIN			
Reviewed					
		VER	SIZE	PAGE	7 OF 9
	V1.0	A4	嘉立创EDA		



Schematic	Schematic1			Update Date	2025-04-28
				Create Date	2025-04-28
Page	RA8875			Part Number	
Drawed		WOLF-MAIN			
Reviewed					
		VER	SIZE	PAGE	8 OF 9
		V1.0	A4	嘉立创EDA	



Schematic	Schematic1			Update Date	2025-04-28	
				Create Date	2025-04-28	
Page	面板			Part Number		
Drawed		WOLF-MAIN				
Reviewed						
		VER	SIZE	PAGE	9	OF 9
		V1.0	A4	嘉立创EDA		