DEFENSE LOGISTICS AGENCY
LAND AND MARITIME
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January 14, 2025

MEMORANDUM FOR MILITARY/INDUSTRY DISTRIBUTION

SUBJECT: Initial Draft of **MIL-PRF-55681H and Supplement 1** (Capacitor, Chip, Multiple Layer, Fixed Ceramic Dielectric, Established Reliability and Non-Established Reliability, General Specification for).

Project number: 5910-2025-008.

The subject document is now available for viewing and downloading from the DLA Land and Maritime - VA website:

https://landandmaritimeapps.dla.mil/Programs/MilSpec/initialdrafts.aspx

This document is being revised to:

- Update the termination finish descriptions in table IV. See CE11 task 18-202.
- Add clarifications to indicate that solderability and resistance to soldering heat testing is applicable to capacitors with solderable terminations only.
- Remove the second DWV measurement from group I of the qualification inspection (see table VIII).
- Update the test frequency requirements for capacitance measurement to match MIL-PRF-23535. See CE11 task 22-302.
- Update board flex and shear stress testing to be in accordance with MIL-STD-202-218 and -219 respectively.
- Add "Intended assembly methods for surface mount capacitors" paragraph to section 6.
- Update the extension of qualification requirements for termination finishes.
- Update the contact information. The Preparing Activity (PA) has been changed from Army-CR to DLA-CC (DLA Land and Maritime).
- Update formatting to meet the accessibility requirements covered by Section 508 of the Rehabilitation Act.

An effort has been made to highlight changes from prior revisions; however, reviewers are cautioned to review the entire document.

Concurrence or comments are required at this Center no later than **17 February 2025**. If comments are not received during the allotted coordination period, concurrence may be assumed. Late comments may be held for the next specification action. Comments from military departments must be identified as either "Essential" or "Suggested". Essential comments must be justified with supporting data. Military review activities should forward comments to their custodians of this office, as applicable, in sufficient time to allow for consolidating the department reply. Since Navy – EC is a custodian for this document; all Navy review activities should forward their comments directly to this Center.

The point of contact for this project is Mr. John Bonitatibus, DLA Land and Maritime - VAT, Post Office Box 3990, Columbus, OH 43218-3990. The preferred method of contact is via email. John can be reached at john.bonitatibus@dla.mil or 614-692-4709/DSN 850-4709.

//Signature on file//

Mark A. Rush
Chief (Acting)
Electronic Components Branch

NOTE: This draft, dated 14 January 2025, prepared by DLA-CC, has not been approved and is subject to modification.
DO NOT USE PRIOR TO APPROVAL. (Project 5910-2025-008)

INCH-POUND
MIL-PRF-55681H~~G~~
~~w/AMENDMENT 1~~
~~8 September 2017~~DRAFT
SUPERSEDING
MIL-PRF-55681G
w/AMENDMENT 1
~~12 July 2016~~8 September 2017

PERFORMANCE SPECIFICATION

CAPACITOR, CHIP, MULTIPLE LAYER, FIXED,
CERAMIC DIELECTRIC, ESTABLISHED RELIABILITY
AND NON-ESTABLISHED RELIABILITY,
GENERAL SPECIFICATION FOR

Termination finish W (see table IV) is inactive for new design after 12 July 2016. For new design, use termination finish Z.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the general requirements for non-established reliability (non-ER) and established reliability (ER), ceramic dielectric, multiple layer, chip capacitors. ER capacitors covered by this specification have failure rate levels (FRL) ranging from 1.0 percent to 0.001 percent per 1,000 hours. These FRLs are established at a 90-percent confidence level and maintained at a 10 percent producer's risk and are based on life tests performed at maximum rated voltage at maximum rated temperature. An acceleration factor of 8:1 has been used to relate life test data obtained at 200 percent of rated voltage at maximum rated temperature, to rated voltage at rated temperature.

1.2 Classification.

1.2.1 Part or Identifying Number (PIN). The PIN is in the following form, and as specified (see 3.1).

CDR01	BX	100	A	K	Z	M
Style (1.2.1.1)	Rated temperature and voltage-temperature limits (1.2.1.2)	Capacitance (1.2.1.3)	Rated voltage (1.2.1.4)	Capacitance tolerance (1.2.1.5)	Termination finish (1.2.1.6)	Product level designator (1.2.1.7)

1.2.1.1 Style. The style is identified by the three-letter symbol "CDR" followed by a two-digit number. The letters identify non-ER and ER, ceramic dielectric, fixed, chip capacitors.

1.2.1.2 Rated temperature and voltage-temperature limits. The rated temperature and voltage-temperature limits are identified by a two-digit symbol. The first letter "B" indicates the rated temperature of -55°C to +125°C; the second letter indicates the voltage-temperature limits as shown in table I.

Comments, suggestions, or questions on this document should be addressed to: DLA Land and Maritime, ATTN: VAT, Post Office Box 3990, Columbus, OH 43218-3990~~CERDEC PRD: RDER-PRO, Building 6010 K-130, Aberdeen Proving Ground, Aberdeen, MD 21005~~, or emailed to: capacitorfilter@dla.mil~~usarmy.apg.cerdec.mbx.standardization-crx@mail.mil~~. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A
FSC 5910

1.2.1.3 Capacitance. The nominal capacitance value expressed in picofarads (pF) is identified by a three-digit number; the first two digits represent significant figures and the last digit specifies the number of zeros to follow. When the nominal value is less than 10 pF, the letter "R" is used to indicate the decimal point and the succeeding digit(s) of the group represent significant figure(s). For example, 1R0 indicates 1.0 pF and 0R5 indicates 0.5 pF.

TABLE I. Voltage-temperature limits.

Symbol	Capacitance change with reference to +25°C		
	Step A through step D of table XIII	Percent rated voltage	Step E through step G of table XIII
G	90 ± 20 ppm/°C	100	90 ± 20 ppm/°C
P 1/	0 ± 30 ppm/°C	100	0 ± 30 ppm/°C
R	± 15 percent	100	+15, -40 percent
X	± 15 percent	100	+15, -25 percent
Z	± 15 percent	60	+15, -45 percent

1/ At measurement point F of table XIII, the capacitance measurement may be ± 0.1 percent or ± 0.05 pF, whichever is greater, from the +25°C reference.

1.2.1.4 Rated voltage. The rated voltage for continuous operation at +125°C is identified by a single letter as shown in table II.

TABLE II. Rated voltage.

Symbol	Rated voltage
V	4
W	6.3
X	10
Y	16
Z	25
A	50
B	100
K	150
C	200
D	300
E	500

1.2.1.5 Capacitance tolerance. The capacitance tolerance is identified by a single letter as shown in table III.

TABLE III. Capacitance tolerance.

Symbol 1/	Capacitance tolerance (±)
B	.10 pF
C	.25 pF
D	.50 pF
F	1 percent
G	2 percent
J	5 percent
K	10 percent
M	20 percent

1/ Symbols B, C, and D are applicable for capacitance values of less than 10 pF only. For capacitance values of .10 pF through .50 pF, the capacitance will never be zero.

1.2.1.6 Termination finish. The termination finish is identified by a single letter as shown in table IV. Only the user should make substitutions.

TABLE IV. Termination finish.

Symbol 1/	Type 2/	Base material	Barrier layer	Final finish
M 3/	Epoxy bondable	--	--	Palladium/silver
N 3/ 4/	Wire or epoxy bondable	Silver	Nickel	Gold
S	Solderable	Silver	--	Solder coated 8/
T	Solderable	--	--	Silver
U 5/	Solderable	Silver	Nickel	Solder coated 8/
W 6/	Solderable	Silver	Nickel	Solder coated 8/
Y 7/	Solderable	Silver	Nickel	Tin (100%)
Z	Solderable	Silver	Nickel	Solder plated 8/

1/ Terminations P (silver-copper-gold) and Q (palladium-gold) are no longer available.
2/ The intended assembly method for each termination style is as noted by type (see 6.14).
3/ Epoxy bondable type terminations are intended to be mounted with a conductive adhesive.
4/ See 6.4.1.
5/ Solder will have a melting point of +200°C or less. Solder coat thickness will be a minimum of 60 micro-inches.
6/ Termination finish W is inactive for new design. Capacitors with termination finish W and date codes prior to 1728 (see 3.23) may contain 100 percent tin and promote tin whisker growth (see 6.4.2). Contact the manufacturer for specific composition.
7/ Termination Y is 100 percent tin and may promote tin whisker growth (see 6.4.2).
8/ Tin/lead alloy with a minimum of 3 percent lead

~~Symbol 1/~~	~~Finish~~
~~M~~	~~Palladium/silver alloy~~
~~N 2/~~	~~Silver - nickel - gold~~
~~S~~	~~Solder coated final with a minimum of 3 percent lead~~
~~T~~	~~Silver~~
~~U~~	~~Base metallization - nickel - solder coated (tin/lead alloy, with a minimum of 3 percent lead) 3/~~
~~W 4/~~	~~Base metallization – nickel - solder coated (tin/lead alloy, with a minimum of 3 percent lead)~~
~~Y 5/~~	~~Base metallization - nickel - tin (100 percent)~~
~~Z~~	~~Base metallization - nickel - solder plated (tin/lead alloy, with a minimum of 3 percent lead)~~

~~1/ Terminations P (silver copper gold) and Q (palladium gold) are no longer available.~~
~~2/ See 6.4.1.~~
~~3/ Solder will have a melting point of +200°C or less. Solder coat thickness will be a minimum of 60 micro-inches.~~
~~4/ Termination finish W is inactive for new design. Capacitors with termination finish W and date codes prior to 1728 (see 3.23) may contain 100 percent tin and promote tin whisker growth (see 6.4.2). Contact the manufacturer for specific composition.~~
~~5/ Termination Y is 100 percent tin and may promote tin whisker growth (see 6.4.2).~~

1.2.1.7 Product level designator. The product level designator is identified by a single letter as shown in table V.

TABLE V. Product level designator.

Symbol	Product level
C	non-ER
M	1.0 1/
P	0.1 1/
R	0.01 1/
S	0.001 1/

1/ FRL (percent per 1,000 hours).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of the documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract (see 6.2).

DEPARTMENT OF DEFENSE SPECIFICATIONS

(See supplement 1 for list of associated specification sheets.)

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202	-	Electronic and Electrical Component Parts~~, Test Methods for~~
MIL-STD-202-103	-	Method 103, Humidity (Steady State)
MIL-STD-202-104	-	Method 104, Immersion
MIL-STD-202-106	-	Method 106, Moisture Resistance
MIL-STD-202-107	-	Method 107, Thermal Shock
MIL-STD-202-108	-	Method 108, Life (at Elevated Ambient Temperature)
MIL-STD-202-208	-	Method 208, Solderability
MIL-STD-202-210	-	Method 210, Resistance to Soldering Heat
MIL-STD-202-211	-	Method 211, Terminal Strength
MIL-STD-202-301	-	Method 301, Dielectric Withstanding Voltage
MIL-STD-202-302	-	Method 302, Insulation Resistance
MIL-STD-202-305	-	Method 305, Capacitance
MIL-STD-690	-	Failure Rate Sampling Plans and Procedures
MIL-STD-790	-	~~Standard Practice for~~ Established Reliability and High Reliability Qualified Products List (QPL) Systems for Electrical, Electronic, and Fiber Optic Parts Specifications

(Copies of these documents are available online at ~~http://quicksearch.dla.mil/~~ https://quicksearch.dla.mil/.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASSOCIATION CONNECTING ELECTRONICS INDUSTRIESIPC INTERNATIONAL (IPC)

J-STD-004IPC J-STD-004	-	Requirements for Soldering Fluxes
J-STD-005IPC J-STD-005	-	Requirements for Soldering Pastes
J-STD-006IPC J-STD-006	-	Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

(Copies of these documents are available online at www.ipc.orghttps://www.ipc.org/.)

SAE INTERNATIONAL (SAE)

SAE EIA-554-1	-	Assessment of Average Outgoing Quality Levels in Parts Per Million (ppm)

(Copies of these documents are available online at www.sae.orghttps://www.sae.org/.)

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC JESD557	-	Statistical Process Control Systems

(Copies of this document are available online at http://www.jedec.orghttps://www.jedec.org/.)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Specification sheets. The individual item requirements shall be as specified herein and in accordance with the applicable specification sheets. In the event of any conflict between requirements of this specification and the specification sheet, the latter shall govern (see 6.2).

3.2 Qualification. Capacitors furnished under this specification shall be products which are authorized by the qualifying activity for listing on the applicable qualified products list (QPL) before contract award. In addition, the manufacturer shall obtain certification from the qualifying activity that the product assurance requirements of 4.2 have been met and are being maintained.

3.3 QPL system. The manufacturer shall establish and maintain a QPL system for parts covered by this specification. Requirements for this system are specified in MIL-STD-690 (ER parts only) and MIL-STD-790. In addition, the manufacturer shall establish a Statistical Process Control (SPC) and Part Per Million (ppm) system that meets the requirements specified in 3.3.1 and 3.3.2.

3.3.1 SPC system. As part of the overall MIL-STD-790 QPL system, the manufacturer shall establish a SPC system that meets the requirements of JEDEC JESD557.

3.3.2 PPM system. As part of the overall MIL-STD-790 QPL system, the manufacturer shall establish a ppm system for assessing the average outgoing quality of lots in accordance with SAE EIA-554-1. Data exclusion, in accordance with SAE EIA-554-1 may be used with approval of the qualifying activity. The ppm system shall identify the ppm rate at the end of each month and shall be based on a six month moving average. Style reporting may include both non-ER and ER style combinations.

3.4 Material. The material shall be as specified herein. However, when a definite material is not specified, a material shall be used which enables the capacitors to meet the performance requirements of this specification. Acceptance or approval of any constituent material shall not be construed as a guarantee of the acceptance of the finished product.

3.4.1 Soldering flux. Soldering flux shall be in accordance with J-STD-004. No acid, acid salts, or type RA fluxes shall be used in preparation for or during soldering.

3.5 Interface and physical dimension requirements. Capacitors shall meet the interface requirements and physical dimensions specified (see 3.1).

3.5.1 Terminations. The terminations shall be of solderable metals or metal alloys. Termination finishes, as identified in 1.2.1.6, shall be as specified (see 3.1).

3.5.1.1 Reprocessing of terminations for solderability enhancement. The manufacturer may reprocess the terminations of capacitors supplied to this specification for the purpose of solderability enhancement, provided the termination process has been approved by the qualifying activity.

3.5.1.1.1 Reprocessing option. If the manufacturer reprocesses the terminations of the capacitors as a part of normal production, or as a corrective action for solderability failure, the reprocessed lot shall be subjected to the group A, subgroup 1, electrical tests.

3.5.2 Electrode parameters. Nickel electrodes shall not be used in capacitors supplied to this specification (see 6.12).

3.6 Voltage conditioning. When tested as specified in 4.8.3, capacitors shall meet the following requirements:

a. Dielectric withstanding voltage (DWV) (at +25°C): Shall be as specified in 3.12, with the following exceptions:

(1) For capacitors with a voltage rating of 500 volts, 200 percent of rated voltage shall be applied.

(2) Not applicable if the optional voltage conditioning was performed at or above 250 percent of rated voltage.

b. Insulation resistance (IR) (at +25°C): Shall be as specified in 3.9.

c. Capacitance (at +25°C): Shall be as specified in 3.7.

d. Dissipation factor (DF) (at +25°C): Shall be as specified in 3.8.

3.7 Capacitance. When measured as specified in 4.8.4, the capacitance shall be within the applicable tolerance specified (see 3.1).

3.8 Dissipation factor. When measured as specified in 4.8.5, the DF shall meet the following:

Characteristic	Maximum allowable DF (%)					
	Rated Voltage (V_{dc})					
	4	6.3	10	16	25	≥50
BR, BX, BZ	7.5	7.5	5.0	3.5	3.5	2.5
BP (≥ 10 pf)	0.15	0.15	0.15	0.15	0.15	0.15
BP (< 10 pf)	0.25	0.25	0.25	0.25	0.25	0.25
BG (≥ 10 pf)	0.05	0.05	0.05	0.05	0.05	0.05
BG (< 10 pf)	0.15	0.15	0.15	0.15	0.15	0.15

3.9 Insulation resistance. When measured as specified in 4.8.6, the IR shall be not less than the following:

a. At +25°C (except high frequency styles) (see 3.1).

(1) Capacitors rated 25 V_{dc} and higher: 100,000 megohms or 1,000 megohm-microfarads, whichever is less.

(2) Capacitors rated less than 25 V_{dc}: 100,000 megohms or 500 megohm-microfarads, whichever is less.

b. At +125°C (except high frequency styles) (see 3.1):

(1) Capacitors rated 25 V_{dc} and higher:

(a) BR, BX, and BZ characteristics: Shall be not less than 10,000 megohms or 100 megohm-microfarads, whichever is less (see 3.1).

(b) BP characteristic: Shall be not less than 1,000 megohms or 10 megohm-microfarads, whichever is less (see 3.1).

(c) BG characteristic: Shall be as specified (see 3.1).

(2) Capacitors rated less than 25 V_{dc}: Shall be not less than 10,000 megohms or 50 megohm-microfarads, whichever is less.

3.10 Equivalent series resistance (ESR) (UHF) (when specified, see 3.1). When tested in accordance with 4.8.7, the ESR shall be less than the limits shown in appendix A, figure A-1, and figure A-2.

3.11 Equivalent series resistance (RF) (when specified, see 3.1). When tested in accordance with 4.8.8, the ESR shall be less than the limits shown in appendix A, figure A-3 and figure A-4.

3.12 Dielectric withstanding voltage. When capacitors are tested as specified in 4.8.9, there shall be no evidence of breakdown or visible evidence of arcing or damage.

3.13 Solderability.

3.13.1 Nonleaded capacitors. Capacitors shall be tested as specified in 4.8.10. Nonbarrier metal capacitors shall utilize Pb36B solder; barrier metal capacitors shall utilize Sn60A, Pb36B, or Sn63A solder (see 3.1) in accordance with J-STD-006, and the immersed metallized surface shall be at least 85 percent covered with a smooth solder coating. The remaining 15 percent of the surface may contain small pinholes or exposed termination material; however, these shall not be concentrated in one area.

3.13.2 Leaded capacitors. When leaded capacitors are tested as specified in 4.8.10, the dipped surface of the leads shall be at least 90 percent covered with a new, smooth solder coating. The remaining 10 percent may contain only small pinholes or rough spots, and these shall not be concentrated in one area. Bare base metal where the solder dip failed to cover the original coating is an indication of poor solderability and shall be cause for failure. In case of dispute, the percentage of coverage with pinholes or rough spots shall be determined by actual measurement of these areas, as compared to the total area.

3.14 Voltage-temperature limits (not applicable to high frequency capacitors). When capacitors are tested as specified in 4.8.11, the capacitance change shall not exceed the applicable limits specified in table I. For BP and BG capacitors of less than 20 pF, the following capacitance change limits shall apply:

Permissible capacitance change from capacitance at +25°C in ppm/°C					
Temperature	Less than 2.1 pF	2.15 pF to 4.2 pF	4.3 pF to 8.0 pF	8.1 pF to 18 pF	Greater than 18 pF
+125°C	1/	± 250 ppm/°C	± 120 ppm/°C	± 60 ppm/°C	± 30 ppm/°C
-55°C 2/	1/	+246.25 -326.25	+116.25 -166.25	+55.00 -91.25	+27.50 -53.75

1/ Not practically measurable.
2/ The ppm/°C values for -55°C were calculated by dividing ppm by -80°C.

3.15 Thermal shock and immersion. When tested as specified in 4.8.12, capacitors shall meet the following requirements:

a. Visual examination: There shall be no mechanical damage.

b. DWV: Shall be as specified in 3.12.

c. IR (at +25°C): Shall be not less than 30 percent of the initial requirement (see 3.9).

d. Capacitance change:

(1) BR, BX, and BZ characteristics: Shall change not more than ±10 percent from the initial measured value.

(2) BG and BP characteristics: Shall change not more than 0.5 percent of the nominal value or 0.5 pF, whichever is greater, from the initial measured value.

e. DF: Shall be as specified in 3.8.

3.16 Resistance to soldering heat. When tested as specified in 4.8.13, capacitors shall meet the following requirements:

a. Visual examination: There shall be no evidence of mechanical damage or delamination or exposed electrodes. Leaching shall be a maximum of 25 percent on each edge of mounting area (see figure 1).

b. IR (at +25°C): Shall not be less than the initial +25°C requirement.

c. Capacitance change:

(1) BR, BX, and BZ characteristics: Shall change not more than -1.0 percent to +6.0 percent from the initial measured value.

(2) BG characteristic: Shall change not more than 0.5 percent of the nominal value or 0.5 pF, whichever is greater, from the initial measured value.

(3) BP characteristic: Shall change not more than -1.0 percent to +2.0 percent of the nominal value or 0.5 pF, whichever is greater, from the initial measured value.

d. DF: Shall not exceed the initial limits.

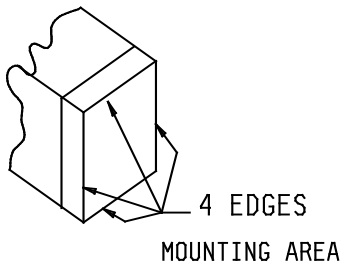


FIGURE 1. Mounting areas.

3.17 Moisture resistance. When tested as specified in 4.8.14, capacitors shall meet the following requirements:

a. Visual examination: There shall be no mechanical damage, and marking shall remain legible.

b. DWV: Shall be as specified in 3.12.

c. IR (at +25°C): Shall be not less than 30 percent of the initial requirement (see 3.9).

d. Capacitance change:

(1) BR, BX, and BZ characteristics: Shall change not more than ±10 percent from the initial measured value.

(2) BP and BG characteristics: Shall change not more than 0.5 percent of the nominal value or 0.5 pF, whichever is greater, from the initial measured value.

3.18 Humidity, steady state, low voltage. When tested as specified in 4.8.15, capacitors shall meet the following requirements:

a. Visual examination: There shall be no mechanical damage, and marking shall remain legible.

b. IR (at +25°C): Shall meet the initial +25°C requirement specified in 3.9.

c. Capacitance change:

(1) BR, BX, and BZ characteristics: Shall not change more than ±10 percent from the initial measured value.

(2) BP and BG characteristics: Shall not change more than 0.3 percent of the nominal value or 0.3 pF, whichever is greater, from the initial measured value.

3.19 Life (at elevated ambient temperature). When tested as specified in 4.8.16, capacitors shall meet the following requirements:

a. Visual examination: There shall be no mechanical damage.

b. IR:

(1) (At +25°C): Shall be not less than 30 percent of the initial requirement (see 3.9).

(2) (At maximum rated temperature): Shall be not less than 30 percent of the initial requirement (see 3.9).

c. Capacitance change:

(1) BR, BX, and BZ characteristics: Less than ±10 percent from the initial measured value.

(2) BP and BG characteristics: Shall change not more than 2.0 percent of the nominal value or 0.5 pF, whichever is greater, from the initial measured value.

d. DF:

(1) BR, BX, and BZ characteristics: Shall not be more than the values specified below:

Rated Voltage (V_{dc})	Maximum DF (%)
≥ 50V	3.0
16V – 25V	5.0
10V	7.5
4V – 6.3V	10

(2) BP and BG characteristics: Less than 0.2 percent.

3.20 Series resonance (when specified, see 3.1). When tested as specified in 4.8.17, capacitors shall meet or exceed the series resonance frequency as shown on figure 2.

3.21 Terminal integrity.

3.21.1 Nonleaded capacitors.

3.21.1.1 Board flex. When tested as specified in 4.8.18.1.1, capacitors shall meet the following:

a. Capacitance:

(1) During examination: Shall change not more than ± 5% for BP and BG characteristics or ± 10% for BR, BX, and BZ characteristics.

(2) After examination: Shall be within the tolerance specified (see 3.1).

b. Dissipation factor: Shall not exceed the initial limit (see 3.8).

c. Visual examination: There shall be no mechanical damage to the capacitor body, terminals, and body/terminal junction.

3.21.1.2 Shear stress. When capacitors are tested as specified in 4.8.18.1.2, there shall be no evidence of cracking or the capacitor being sheared from its pad.

3.21.2 Leaded capacitors.

3.21.2.1 Terminal strength. When capacitors are tested as specified in 4.8.18.2.1, there shall be no loosening, rupturing, or permanent damage to the terminals.

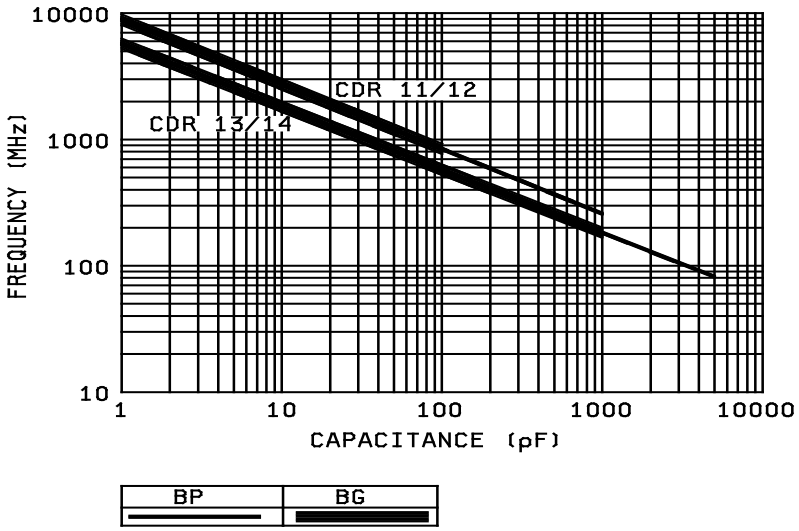


FIGURE 2. Series resonance frequency versus nominal capacitance value.

3.22 Temperature coefficient and capacitance drift (high frequency capacitors only).

3.22.1 Temperature coefficient. When capacitors are tested as specified in 4.8.19, the capacitance change shall not exceed the applicable limits specified in table I.

PPM per °C can be calculated with the following equation:

$$Temperature\ coefficient\ (ppm/°C) = \frac{C_2 - C_1}{C_1(T_2 - T_1)} * 10^6$$

where: C_2 = Capacitance at test temperature
C_1 = Capacitance at +25°C
T_2 = Test temperature
T_1 = +25°C

3.22.2 Capacitance drift. The capacitance drift shall be within ± (0.2 percent or 0.05pF), whichever is greater.

3.23 Marking.

3.23.1 Marking (all styles except high frequency). Packaging containers shall be marked with the PIN (see 1.2.1), capacitance, capacitance tolerance, voltage, "JAN" brand, lot symbol, date code, and the Commercial and Government Entity (CAGE) code. The date code shall consist of the year and week (e.g. week 40 of 2005 would be 0540). Other markings which in any way interfere with, obscure, or confuse those specified herein are prohibited. When specified in the ordering data (see 6.2), capacitor sizes 0805 and larger shall be legibly marked in accordance with either of the two options below:

a. Option A: In accordance with table VI.

b. Option B: In accordance with table VII using a two character system. The first character shall be an alphabetic symbol and shall designate the first and second significant figures. The second character shall be a numerical digit and shall designate the decimal multiplier of capacitance in pF (Examples: A1 = 1 x 10^1 = 10 pF; J5 = 2.2 x 10^5 = 0.22 x 10^6 = 0.22 μF). The marking shall appear in black or legible contrast. The size and orientation of the marking shall be at the option of the manufacturer. At the option of the manufacturer, the capacitor may be laser marked with the manufacturer's trademark or symbol and the capacitance code in accordance with table VII.

Additional marking may appear provided that it does not interfere with the required marking.

TABLE VI. Color marking for capacitors.

Character	Significant units	Capacitance (pF) and multiplier					
		Orange (x 0.1)	Black (x 1.0)	Green (x 10)	Blue (x 100)	Violet (x 1000)	Red (x 10,000)
A	10	1.0	10	100	1000	10,000	100,000
B	11	1.1	11	110	1100	11,000	110,000
C	12	1.2	12	120	1200	12,000	120,000
D	13	1.3	13	130	1300	13,000	130,000
E	15	1.5	15	150	1500	15,000	150,000
H	16	1.6	16	160	1600	16,000	160,000
I	18	1.8	18	180	1800	18,000	180,000
J	20	2.0	20	200	2000	20,000	200,000
K	22	2.2	22	220	2200	22,000	220,000
L	24	2.4	24	240	2400	24,000	240,000
N	27	2.7	27	270	2700	27,000	270,000
O	30	3.0	30	300	3000	30,000	300,000
R	33	3.3	33	330	3300	33,000	330,000
S	36	3.6	36	360	3600	36,000	360,000
T	39	3.9	39	390	3900	39,000	390,000
V	43	4.3	43	430	4300	43,000	430,000
W	47	4.7	47	470	4700	47,000	470,000
X	51	5.1	51	510	5100	51,000	510,000
Y	56	5.6	56	560	5600	56,000	560,000
Z	62	6.2	62	620	6200	62,000	620,000
3	68	6.8	68	680	6800	68,000	680,000
4	75	7.5	75	750	7500	75,000	750,000
7	82	8.2	82	820	8200	82,000	820,000
9	91	9.1	91	910	9100	91,000	910,000

TABLE VII. Two-character marking for chip capacitors.

First character				Second character	
Alphabetic character	Significant figures	Alphabetic character	Significant figures	Numerical character	Decimal multiplier
A	1.0	T	5.1	0	10^0
B	1.1	U	5.6	1	10^1
C	1.2	V	6.2	2	10^2
D	1.3	W	6.8	3	10^3
E	1.5	X	7.5	4	10^4
F	1.6	Y	8.2	5	10^5
G	1.8	Z	9.1	6	10^6
H	2.0	a	2.5	7	10^7
J	2.2	b	3.5	8	10^8
K	2.4	d	4.0	9	10^9
L	2.7	e	4.5		
M	3.0	f	5.0		
N	3.3	m	6.0		
P	3.6	n	7.0		
Q	3.9	t	8.0		
R	4.3	y	9.0		
S	4.7				

3.23.2 Marking (styles CDR11, CDR12, CDR13, CDR14, CDR21, CDR22, CDR23, CDR24, and CDR25). Packaging containers shall be marked with the PIN (see 1.2.1), capacitance, capacitance tolerance, voltage, "JAN" brand, lot symbol, date code, and the Commercial and Government Entity (CAGE) code. The date code shall consist of the year and week (e.g. week 40 of 2005 would be 0540). Other markings which in any way interfere with, obscure, or confuse those specified herein are prohibited. The capacitors shall be marked with a contrasting color dot placed on the side of the capacitor to indicate the vertical plate orientation to that side. At the option of the manufacturer, capacitors may be laser or ink marked with the manufacturer's trademark or symbol, the two-digit or three-digit capacitance code, and the tolerance code as shown in figure 3. ~~When parts are laser marked, t~~The marking shall be on the surface which is parallel to the plane of the embedded electrodes (this is the larger area which is normally the imprint area). If the capacitor is so marked, the vertical plate orientation is defined; therefore, the contrasting color dot on the capacitor to indicate the vertical plate orientation to that side may be an option.

~~Capacitors may be laser marked with the manufacturer's trademark or symbol, the two-digit or three-digit capacitance code, and the tolerance code as follows:~~

~~XXX~~
~~100 (or A1 for two-digit)~~
~~F~~

~~or~~

~~XXX~~
~~100F (or A1F for two-digit)~~

NOTE:
1. Where space does not permit, the manufacturer's trademark or symbol may be omitted.
2. The marking may be 1, 2, or 3 lines as shown.

FIGURE 3. Optional marking for styles CDR11, CDR12, CDR13, CDR14, CDR21, CDR22, CDR23, CDR24, and CDR25.

3.23.3 Substitutability of product levels. A manufacturer may supply to those product levels, as listed below, with failure rates (FR) higher than that to which they are qualified. Parts with lower FRs are substitutable, with the user's approval, for higher FR parts, provided the lot date codes of the parts are not changed.

Parts qualified to product level	Are substitutable for product level
S (.001)	C, M, P, and R
R (.01)	C, M, and P
P (.1)	C, M
M (1)	C
C	NA

3.23.4 Substitutability of capacitance tolerance and rated voltage. Parts qualified and marked (if applicable) to tighter capacitance tolerance or qualified to a higher rated voltage are substitutable, with the user's approval, for parts qualified and marked (if applicable) to looser capacitance tolerance, or qualified to a lower rated voltage, provided all other values, such as case size, characteristic, and leads or terminations remain the same. The substitutable parts shall not be remarked (if applicable) unless specified in the contract or order (see 6.2). In the event the capacitance tolerance is changed and remarked (if applicable) or the voltage rating is changed, the lot date codes of the parts shall not be changed and the workmanship criteria shall be met.

3.23.5 JAN and J marking. The United States Government has adopted and is exercising legitimate control over the certification marks “JAN” and “J”, respectively, to indicate that items so marked or identified are manufactured to, and meet all the requirements of specifications. Accordingly, items acquired to, and meeting all of the criteria specified herein and in applicable specifications shall bear the certification mark “JAN” except that items too small to bear the certification mark “JAN” shall bear the letter “J”. The “JAN” or “J” shall be placed immediately before the part number except that if such location would place a hardship on the manufacturer in connection with such marking, the “JAN” or “J” may be located on the first line above or below the part number. Items furnished under contracts or orders which either permit or require deviation from the conditions or requirements specified herein or in applicable specifications shall not bear “JAN” or "J". In the event an item fails to meet the requirements of this specification and the applicable specification sheets, the manufacturer shall remove completely the military part number and the “JAN” or the “J” from the sample tested and also from all items represented by the sample. The “JAN” or “J” certification mark shall not be used on products acquired to contractor drawings or specifications. The United States Government has obtained Certificate of Registration Number 6,069,576~~504,860~~ for the certification mark “JAN” and Registration Number 2,577,735 for the certification mark “J”.

3.24 Recycled, recovered, environmentally preferable, or biobased materials. Recycled, recovered, environmentally preferable, or biobased materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.25 Workmanship. Capacitors shall be inspected to the criteria in appendix C.

4. VERIFICATION

4.1 Classification of inspections. The inspections specified herein are classified as follows:

a. Qualification inspection (see 4.4).

b. Verification of qualification (see 4.5).

c. Conformance inspection (see 4.6).

d. Periodic group C inspection (see 4.7).

4.2 QPL system. The manufacturer shall establish and maintain a system to meet the requirements of MIL-STD-790 and the requirements herein (see 3.3). Evidence of such compliance shall be verified by the qualifying activity as a prerequisite for qualification and retention of qualification.

4.3 Inspection conditions and methods.

4.3.1 Inspection conditions. Unless otherwise specified herein, all inspections shall be performed in accordance with the test conditions specified in the "GENERAL REQUIREMENTS" of MIL-STD-202.

4.3.2 Methods.

4.3.2.1 Reference measurements. When requirements are based on comparative measurements made before and after conditioning, the reference measurement shall be considered the last measurement made at +25°C ± 5°C prior to conditioning. Unless reference measurements have been made within 30 days prior to the beginning of conditioning, they shall be repeated.

4.3.3 Power supply. The power supply used for life testing shall have a regulation of ± 2 percent, or less, of the applicable applied test voltage. The power supply used for IR measurements shall be stabilized to at least ± 100 ppm. No voltage fluctuations shall occur during measurements that would produce a variation in the current or resistance measurement.

4.4 Qualification inspection. Qualification inspection shall be performed at a laboratory acceptable to the Government (see 6.3) on sample units produced with equipment and procedures normally used in production.

4.4.1 Sample size. The number of sample units comprising a sample of capacitors to be submitted for qualification inspection shall be as specified in table VIII, or in appendix B to this specification. The sample shall be taken from a production run and shall be produced with equipment and procedures normally used in production.

4.4.2 Inspection routine. Sample units shall be subjected to the qualification inspection specified in table VIII, in the order shown. All sample units shall be subjected to the group I tests. These sample units shall then be divided as shown in table VIII for groups II through VIII, and subjected to the tests for their particular group.

4.4.3 Failures. Failures in excess of those allowed in table VIII shall be cause for refusal to grant qualification approval.

4.4.4 FRL and quality level verification.

4.4.4.1 FR qualification and lot conformance FR inspection. FR qualification and lot conformance FR inspection shall be in accordance with the general and detailed requirements of MIL-STD-690 and the following details:

a. Procedure I: Qualification at the initial FR level. Level M (1.0 percent) of FRSP-90 shall apply. Sample units shall be subjected to the qualification inspection specified in group V, table VIII (see 4.4.2).

b. Procedure II: Extension of qualification to lower FR levels. To extend qualification to the P (0.1 percent), R (0.01 percent), and S (0.001 percent) FR levels, two or more voltages within a style and of similar construction may be combined. For FR levels R and S, two or more styles of similar construction (see 4.6.1.1.1) may be combined.

c. Procedure III: Maintenance of FR level qualification. Maintenance period B of FRSP-10 shall apply. Regardless of the number of production lots produced during this period, the specified number of unit hours shall be accumulated to maintain qualification.

4.4.4.2 Quality level verification. The manufacturer is responsible for establishing a quality system to assess the ppm defect level of lots. The ppm defect level shall be based on a 6-month moving average. The following groupings of styles shall be used for the maintenance of ppm defect level:

Group	Styles
1	CDR01, CDR02, CDR03, CDR04, CDR05, CDR06, CDR31, CDR32, CDR33, CDR34, CDR35, CDR36, CDR37
2	CDR11, CDR12, CDR13, CDR14, CDR21, CDR22, CDR23, CDR24, CDR25

TABLE VIII. Qualification inspection.

Inspection	Requirement paragraph	Test method paragraph	Number of sample units to be inspected	Number of defectives permitted
Group I				
Voltage conditioning	3.6	4.8.3		
DWV 1/	3.12	4.8.9		
IR (elevated temperature) 1/	3.9	4.8.6		
Capacitance 1/	3.7	4.8.4		
Dissipation factor 1/	3.8	4.8.5		
IR 1/	3.9	4.8.6	97 5/	Not applicable
ESR (UHF) (high frequency styles only) 2/	3.10	4.8.7		
ESR (RF) (high frequency styles only) 2/	3.11	4.8.8		
~~DWV~~	~~3.12~~	~~4.8.9~~		
Visual and mechanical examination	3.1, 3.4, 3.5.1, 3.23 thru 3.25	4.8.2		
Group II				
Solderability (solderable terminations only (see table IV)	3.13	4.8.10	6	
Group III				
Voltage-temperature limits 3/	3.14	4.8.11		
Temperature coefficient and capacitance drift (high frequency styles only)	3.22	4.8.19	18	1
Thermal shock and immersion	3.15	4.8.12		
Group IV				
Resistance to soldering heat (solderable terminations only (see table IV)	3.16	4.8.13	9	
Moisture resistance	3.17	4.8.14	9	
Group V				
Life (at elevated ambient temperature)	3.19	4.8.16	25	1
Group VIa (leaded capacitors only)				
Series resonance (high frequency only) 2/	3.20	4.8.17	18	0
Terminal strength	3.21.2.1	4.8.18.2.1		
Group VIb (nonleaded capacitors only)				
Series resonance (high frequency only) 2/	3.20	4.8.17		
Board flex	3.21.1.1	4.8.18.1.1	18 4/	0
Shear stress	3.21.1.2	4.8.18.1.2		
Group VII				
Humidity, steady state, low voltage	3.18	4.8.15	12	0

1/ Performed as part of the voltage conditioning test.
2/ Not applicable to high frequency styles below 1 pF.
3/ Not applicable to high frequency capacitors.
4/ Following the series resonance test, if applicable (see 3.1), the samples shall be divided evenly for the board flex and shear stress tests.
5/ 91 for wire or epoxy bondable terminations (see table IV).

4.5 Verification of qualification. Every 12 months, the manufacturer shall provide verification of qualification to the qualifying activity. Continuation of qualification shall be based on meeting the following requirements:

a. MIL-STD-790 program.

b. The capacitor design has not been modified.

c. Lot rejection for group A inspection does not exceed 10 percent or one lot, whichever is greater.

d. Periodic group C inspection.

e. Verification of FRLs.

f. PPM assessment. This information shall be submitted in accordance with style groupings listed in 4.4.4.2.

g. Continued qualification to non-ER (C level) shall be based upon continued maintenance of qualification for the ER part (FRL P).

In the event that there is no production of a single style device during a maintenance period and the manufacturer is listed for more than one style on the QPL, a report shall be submitted certifying that the manufacturer still has the capabilities and facilities necessary to produce that product. However, the manufacturer shall still maintain the required number of unit hours in the maintenance period using those styles produced in order to remain qualified to the applicable FRL. In the case where the lowest FR for an unproduced style is M, styles need not be manufactured for testing only but the manufacturer must certify that the capability and facilities needed to produce that style are still in place. In the event that units must be built for the purpose of maintaining the required hours, they shall also undergo all required testing prior to being placed on life test. If, during two consecutive reporting periods, there has been no production of a given style, the manufacturer may be required, at the discretion of the qualifying activity, to submit a newly-produced (not from stock) representative product of that style to testing.

4.6 Conformance inspection.

4.6.1 Inspection of product for delivery. Inspection of product for delivery shall consist of group A inspection.

4.6.1.1 Inspection and production lot.

4.6.1.1.1 Inspection lot. An inspection lot shall consist of all capacitors of the same voltage-temperature characteristic, produced under essentially the same conditions with the same basic materials, and offered for inspection at one time. The samples selected from the inspection lot shall be representative of the capacitance values and voltages in the approximate ratio of production.

4.6.1.1.2 Production lot. A production lot shall consist of all capacitors of the same style, voltage rating, nominal capacitance value, voltage-temperature characteristic, and termination finish. Manufacture of all parts in the lot shall have been started, processed, assembled, and tested as a group. Lot identity shall be maintained throughout the manufacturing cycle. Non-ER and ER lots, for conformance testing, shall be kept separate.

4.6.1.2 Group A inspection.

4.6.1.2.1 Non-ER capacitors (C-level). The manufacturer shall establish and maintain an inspection system to verify that capacitors meet the capacitance, DF, IR (at +25°C), visual/mechanical, and solderability requirements. In-line or process control may be part of such system. The inspection system shall also include criteria for lot rejection and corrective actions. The inspection system shall be verified under the overall MIL-STD-790 QPL system. NOTE: Since the non-ER (C-level) is the ER design without the mandatory conformance inspection and FRL assessment, this product is still expected to meet the environmental qualification type requirements (e.g., moisture resistance, thermal shock, etc).

4.6.1.2.2 ER capacitors. Group A inspection shall consist of the examinations and tests specified in table IX.

4.6.1.2.3 Subgroup 1 test. Subgroup 1 test shall be performed on a production lot basis on 100 percent of the product supplied under this specification. Capacitors failing the tests of subgroup 1 shall be removed from the lot. If during the 100 percent inspection, screening requires that more than 8 percent of the capacitors be discarded, the entire production lot shall be rejected.

4.6.1.2.3.1 Manufacturer's production inspection. If the manufacturer performs tests equal to or more stringent than those specified in subgroup 1, table IX, as the final step of the production process, group A, subgroup 1 inspection may be waived. Authority to waive the subgroup 1 inspection shall be granted by the qualifying activity only. The following criteria shall be complied with:

a. Tests conducted by the manufacturer during production shall be clearly identical to or more stringent than that

specified for subgroup 1. Test conditions shall be equal to or more stringent than those specified for subgroup 1 tests. (NOTE: Includes optional voltage conditioning (see 4.8.3.2)).

b. Manufacturer subjects 100 percent of the product supplied under this specification to his production tests.

c. The parameters measured and the failure criteria shall be the same or more stringent than those specified herein.

d. The lot rejection criteria is the same or more stringent than that specified herein.

e. Once approved, the manufacturer shall not change the test procedures or criteria without prior notification and concurrence by the qualifying activity.

4.6.1.2.3.2 Rejected lots. Production lots exceeding the eight percent defective allowance (PDA) of group A, subgroup 1 inspection shall be segregated from new lots and lots that have passed inspection. Lots rejected may be offered for acceptance only if the manufacturer 100 percent retests to the requirements of subgroup 1. Resubmitted lots shall be kept separate and shall be clearly identified as resubmitted lots. If, during the 100 percent reinspection to subgroup 1, the lot exceeds 3 percent defective, the lot shall be rejected and shall not be resubmitted.

TABLE IX. Group A inspection.

Inspection	Requirement paragraph	Test method paragraph	Sampling procedure
Subgroup 1			
Voltage conditioning 1/	3.6	4.8.3	100 percent inspection
Subgroup 2			
IR (elevated temperature) (+125°C)	3.9	4.8.6	Table X, column A
Visual and mechanical examination 2/	3.1, 3.4, 3.5, 3.5.1, 3.23 through 3.25	4.8.2	Table X, column B
Subgroup 3			
ESR (UHF) (when specified, see 3.1) 3/	3.10	4.8.7	6 samples
ESR (RF) (when specified, see 3.1) 3/	3.11	4.8.8	0 failures
Subgroup 4			
Solderability (solderable terminations only (see table IV) 4/	3.13	4.8.10	13 samples 0 failures

1/ For CDR11 through CDR14 and CDR21 through CDR25 capacitors of less than 10 pF, the DF shall not exceed 0.25 percent for the BP characteristic and 0.15 percent for the BG characteristic. A negative reading is not considered a failure.
2/ The manufacturer may request the deletion of the subgroup 2, visual and mechanical examination, provided an in-line or process control system for assessing and assuring the visual and mechanical requirements are met, can be validated and approved by the qualifying activity. Deletion of this examination does not relieve the manufacturer from meeting these requirements.
3/ Not applicable to styles CDR11 through CDR14 and CDR21 through CDR25 below 1 pF.
4/ The manufacturer may request the deletion of the subgroup 4 solderability test, provided an in-line or process control system for assessing and assuring the solderability of leads can be validated and approved by the qualifying activity. Deletion of the test does not relieve the manufacturer from meeting this test requirement.

4.6.1.2.4 Subgroup 2 tests.

4.6.1.2.4.1 Sampling plans. Subgroup 2 tests shall be performed on an inspection lot basis. Samples subjected to subgroup 2 shall be selected in accordance with table X, based on the size of the inspection lot. In the event of one or more failures the lot shall be rejected.

4.6.1.2.4.2 Rejected lots. The rejected lot shall be segregated from new lots and those lots that have passed inspection. The rejected lot shall be 100 percent inspected for those quality characteristics found defective in the sample and any defectives found removed from the lot. A new sample of parts shall then be randomly selected in

accordance with table X. If one or more defects are found in this second sample, the production lot shall be rejected and shall not be supplied to this specification.

TABLE X. Sampling plans for subgroup 2.

Lot size	Sample Size	
	A	B
1 - 13	100%	100%
14 - 125	100%	13
126 - 150	125	13
151 - 280	125	20
281 - 500	125	29
501 - 1,200	125	34
1,201 - 3,200	125	42
3,201 - 10,000	192	50
10,001 - 35,000	294	60
35,001 - 150,000	294	74
150,001 - 500,000	345	90
500,001 - up	435	102

4.6.1.2.5 Subgroup 3 tests. Subgroup 3 shall be performed on an inspection lot basis. The sampling procedure shall be as specified in table IX.

4.6.1.2.5.1 Rejected lots. The rejected lots shall be segregated from new lots and those lots that have passed inspection. Lots rejected because of failures in subgroup 3 shall be re-inspected, using the sampling procedure specified in table IX. If one or more defects are found in the second sample, the lot shall be rejected and shall not be supplied to this specification. Resubmitted lots shall be kept separate from new lots, and shall be identified as resubmitted lots.

4.6.1.2.6 Subgroup 4 (solderability).

4.6.1.2.6.1 Sampling plan. Thirteen samples shall be selected randomly from every inspection lot and subjected to the subgroup 4 solderability test. The manufacturer may use electrical rejects from the subgroup 1 screening tests for all or part of the samples to be used for the solderability testing. If there are one or more defects, the lot shall be considered to have failed.

4.6.1.2.6.2 Rejected lots. In the event of one or more defects, the inspection lot shall be rejected. The manufacturer may use one of the following options to rework the lot:

a. Each production lot that was used to form the failed inspection lot shall be individually submitted to the solderability test as required in 4.6.1.2.6.1. Production lots failing the solderability test can be reworked only if submitted to the reprocessing procedure in 4.6.1.2.6.2b.

b. The manufacturer shall submit the failed production lot to 100 percent reprocessing of the terminations, using a process approved by the qualifying activity. Following the reprocessing, the electrical measurements required in the group A, subgroup 1 test shall be repeated on 100 percent of the lot. The PDA for electrical measurements shall be as for the subgroup 1 tests. Thirteen additional samples shall then be selected and subjected to the solderability test with no defects allowed. If the lot fails this solderability test, the lot shall be considered rejected and shall not be furnished against the requirements of this specification.

4.6.1.2.6.3 Disposition of samples. The solderability test is considered a destructive test and samples submitted to the solderability test shall not be supplied on the contract.

4.6.1.2.7 PPM calculations. The manufacturer shall establish a ppm system in accordance with 3.3.2 for assessing and calculating average outgoing quality of capacitors. A ppm rate combining capacitance, DF, IR (+25°C), and DWV shall be assessed for lots that have passed the group A inspection. The manufacturer's ppm

system shall also address rectification procedures for lots failing ppm assessment. Data from the rectification process shall not be used to calculate ppm.

4.7 Periodic group C inspection (ER only). Periodic inspection shall consist of the group C inspection tests specified in table XI, in the order shown. Group C inspection shall be performed on sample units randomly selected from inspection lots which have passed group A inspection. Except where the results of periodic inspection show noncompliance with the applicable requirements (see 4.7.2), delivery of products which have passed group A inspection shall not be delayed pending the results of this periodic inspection.

TABLE XI. Group C inspection.

Inspection	Requirement paragraph	Test method paragraph	Number of sample units to be inspected	Number of defectives permitted
Subgroup 1				
Temperature coefficient and capacitance drift	3.22	4.8.19		
Voltage-temperature limits 1/ 2/	3.14	4.8.11	12	0
Thermal shock and immersion 3/	3.15	4.8.12		
Subgroup 2				
Resistance to soldering heat (solderable terminations only (see table IV)	3.16	4.8.13	12	0
Moisture resistance	3.17	4.8.14		
Subgroup 3				
Life (at elevated ambient temperature)	3.19	4.8.16	25 minimum	See 4.7.1.2
Subgroup 4a (leaded capacitors only)				
Series resonance (high frequency only) 5/	3.20	4.8.17	12	0
Terminal strength 3/	3.21.2.1	4.8.18.2.1		
Subgroup 4b (nonleaded capacitors only)				
Series resonance (high frequency styles only) 5/	3.20	4.8.17	12 4/	0
Board flex 3/	3.21.1.1	4.8.18.1.1		
Shear stress 3/	3.21.1.2	4.8.18.1.2		
Subgroup 5				
Humidity, steady state, low voltage	3.18	4.8.15	12	0

1/ If the manufacturer can demonstrate that this test has been performed five consecutive times with zero failures, the frequency of this test, with the approval of the qualifying activity, can be performed on an annual basis. If the design, material, construction or processing of the part is changed or, if there are any quality problems or failures, the qualifying activity may require resumption of the original test frequency.
2/ Not applicable to high frequency capacitors.
3/ If the manufacturer can demonstrate that this test has been performed five consecutive times with zero failures, this test, with the approval of the qualifying activity, can be deleted. The manufacturer, however, shall perform this test every three years after the deletion as part of long term design verification. If the design, material, construction or processing of the part is changed or, if there are any quality problems, the qualifying activity may require resumption of the specified testing. Deletion of testing does not relieve the manufacturer from meeting the test requirement in case of dispute.
4/ Following the series resonance test, if applicable (see 3.1), the samples shall be divided evenly for the board flex and shear stress tests.
5/ Not applicable to high frequency styles below 1 pF.

4.7.1 Sampling plan.

4.7.1.1 Subgroup 1, subgroup 2, and subgroup 5 (all FR levels). Thirty-six sample units of each voltage-temperature characteristic shall be randomly selected from inspection lots (see 4.6.1.1.1) that have passed the group A inspection every 6 months.

4.7.1.2 Subgroup 3 (all FR levels). A minimum of 25 sample units per style of the highest capacitance value produced shall be randomly selected from inspection lots (see 4.6.1.1.1) that have passed the group A inspection

every six months. Permitted failures shall be as specified in MIL-STD-690. The accumulated data shall be used for maintenance and extension of FR qualification.

4.7.1.3 Subgroup 4a and subgroup 4b (all FR levels). Twelve sample units shall be selected from inspection lots (see 4.6.1.1.1) that have passed the group A inspection every 6 months.

4.7.1.4 Disposition of sample units. Sample units which have been subjected to group C inspection shall not be delivered on the contract or order.

4.7.2 Noncompliance. If a sample fails to pass group C inspection, the manufacturer shall notify the qualifying activity and cognizant inspection activity of such failure and take corrective action on the materials or processes, or both, as warranted, and on all units of product which can be corrected and which were manufactured under essentially the same conditions, with essentially the same materials and processes, and which are considered subject to the same failure. Acceptance and shipment of the product shall be discontinued until corrective action, acceptable to the qualifying activity has been taken. After the corrective action has been taken, group C inspection shall be repeated on additional sample units (all inspection, or the inspection which the original sample failed, at the option of the qualifying activity). Group A inspection may be reinstituted; however, final acceptance and shipment shall be withheld until the group C inspection has shown that the corrective action was successful.

4.8 Methods of inspection.

4.8.1 Mounting for testing. When specified in the test procedures, the chip capacitors shall be mounted on a suitable substrate (e.g., 96 percent alumina or FR4 glass epoxy). The substrate and mounting process shall be such that it will not be the cause of, nor contribute to, failure of any test for which it may be used. The capacitors shall be mounted on the substrate as follows:

a. A substrate shall be prepared with metallized surface land areas of proper spacing to permit mounting of chips by soldering the terminations of the chips to the substrate land areas. The dimensions of the test card are optional.

b. Solder paste, type Sn60A, Pb36B, or Sn63A in accordance with J-STD-005 and J-STD-006, shall be used.

c. The chip capacitor shall be soldered to the substrate using a solder reflow process. Conductive belt reflow and IR reflow processes are suggested. The temperature range of the peak reflow temperature shall be between +220°C and +260°C. Recommended ramp rates during preheating should not exceed 4°C per second. The substrates and capacitors shall be allowed to cool at room temperature.

d. The substrate shall be cleaned to remove flux residue, if applicable. Any residue which degrades capacitor electrical performance shall be removed.

4.8.1.1 Test rack. When specified, the substrate shall be mounted on a test rack that shall be so designed as to permit readout for electrical parameters at +25°C and +125°C and to monitor each capacitor under test for failure. This will insure uniform and uninterrupted voltage and heat stresses.

4.8.2 Visual and mechanical inspection. Capacitors shall be examined to verify that the materials, design, construction, physical dimensions, and workmanship are in accordance with the applicable requirements (see 3.1, 3.4, 3.5, and 3.23 through 3.25).

4.8.3 Voltage conditioning (see 3.6). One of the voltage conditioning tests in 4.8.3.1 or 4.8.3.2 shall be performed. The lot traveler shall indicate which test is used. When the optional voltage conditioning test of 4.8.3.2 is used, the traveler shall include the specific accelerated voltage used and the test time.

4.8.3.1 Standard voltage conditioning. A minimum of twice the rated voltage shall be applied to the unit at the maximum rated temperature +4°C, -0°C for 100 hours +25 hours, -4 hours. After completion of the exposure period, the unit shall be stabilized at room temperature and the DWV (see 3.6a), IR, capacitance, and DF shall be measured as specified in 4.8.9, 4.8.6, 4.8.4, and 4.8.5, respectively. Due to the deaging characteristic of ceramic, capacitance measurement may be delayed (applicable to BR, BX, and BZ characteristics only).

4.8.3.2 Optional voltage conditioning (capacitors with voltage ratings of 200 volts or less only). The manufacturer, with approval from the qualifying activity, may perform an optional voltage conditioning test instead of the standard voltage conditioning test of 4.8.3.1. All conditions of 4.8.3.1 apply, with the exception of the voltage applied and the test time. The minimum time duration, T_{test}, shall be calculated as follows:

$$T_{test} = \frac{800}{(E_{test}/E_{rated})^3}$$

Where: $2 \times E_{rated} \leq E_{test} \leq 4 \times E_{rated}$
T_{test} = Minimum test time in hours
E_{test} = Applied voltage
E_{rated} = Rated voltage of the capacitor

4.8.4 Capacitance (see 3.7) (for high frequency styles, see 3.1). Capacitors shall be tested in accordance with MIL-STD-202-305. The following details and exception shall apply:

a. Test frequency: 1 MHz ± ~~50~~100 kHz (for all BP and BG characteristic capacitors ≤ 1,000 pF, and for all BX characteristic capacitors ≤ 100 pF); or 1 kHz ± ~~50~~100 Hz for all other capacitors. At the option of the manufacturer, the capacitance measurement of a 100 pF class II capacitor may be performed at either 1 MHz ± 100 kHz or 1 kHz ± 100 Hz.

b. Test voltage: 1.0 volt ± 0.2 volt rms.

Stable capacitance standards may be used, at the option of the manufacturer, to eliminate or reduce capacitance bridge and fixturing error when measuring capacitance of less than 100 pF. The method used for making these measurements shall be included in the manufacturer's program plan in accordance with MIL-STD-790.

4.8.5 Dissipation factor (see 3.8). DF shall be measured with a bridge or other suitable equipment at the frequency and voltage specified in 4.8.4.

4.8.6 Insulation resistance (see 3.9). Capacitors shall be tested in accordance with MIL-STD-202-302. The following details shall apply:

Precautionary note: Prior to performing this test, capacitors shall be carefully cleaned to remove any contamination including fingerprints. Care must be taken to maintain cleanliness in test chamber and while making measurements.

a. Test conditions: Rated voltage as specified (see 3.1) applied through a series resistor sufficient to limit the charging current to a maximum of 50 milliamperes (mA).

b. Special conditions: If a failure occurs at a relative humidity above 50 percent, the IR may be measured again at any relative humidity less than 50 percent.

c. Points of measurement: Between the terminations (metallized ends) or leads.

4.8.7 Equivalent series resistance (UHF) (when specified, see 3.1) (see 3.10). The UHF ESR shall be measured in accordance with appendix A and table XII. Leaded devices shall be characterized as having the same ESR as equivalent nonleaded devices manufactured from the same dielectric/metallization material lot.

TABLE XII. ESR (UHF) test frequency range.

Capacitance range	Frequency range	Wavelength
100 pF or less	910 MHz -1,050 MHz	7/4
101 pF - 330 pF	640 MHz - 660 MHz	5/4
331 pF - 1,000 pF	380 MHz - 400 MHz	3/4

4.8.8 Equivalent series resistance (RF) (when specified, see 3.1) (see 3.11). The RF ESR shall be measured in accordance with appendix A at one-quarter wavelength in a frequency range of 130 MHz to 260 MHz. Leaded devices shall be characterized as having the same ESR as equivalent nonleaded devices manufactured from the same dielectric/metallization material lot.

4.8.9 Dielectric withstanding voltage (see 3.12). Unmounted capacitors shall be tested in accordance with MIL-STD-202-301. The following details and exceptions shall apply:

a. Magnitude and nature of test voltage: Unless otherwise specified (see 3.1), 250 percent of rated voltage.

b. Duration of application of test voltage: 5 seconds ± 1 second.

c. Points of application of test voltage: Unless otherwise specified (see 3.1), between the capacitor-element terminals.

d. Limiting value of surge current: Shall not exceed 50 mA.

e. Examination after test: Capacitors shall be examined for evidence of damage and breakdown.

4.8.10 Solderability (see 3.13). Capacitors shall be tested in accordance with MIL-STD-202-208. The following details and exceptions shall apply:

a. For capacitors without leads, each terminal shall be immersed to a depth of .020 inch +.010 inch, -.000 inch (0.51 mm +0.25 mm, -0.00 mm), or the entire capacitor may be immersed.

b. For capacitors with leads, each terminal shall be immersed to a distance of .030 inch ±.020 inch (0.76 mm ± 0.51 mm) to the capacitor body.

c. Examination of terminations shall be in accordance with 3.13. In case of dispute, the percent coverage with pinholes or rough spots shall be determined by actual measurement of these areas, as compared to the total area.

4.8.11 Voltage-temperature limits (not applicable to high frequency capacitors) (see 3.14). The temperature of each capacitor shall be varied as specified in table XIII. Capacitance measurements shall be made at the frequency specified in 4.8.4. The dc rated voltage need only be applied to the capacitor in each of step E through step G until voltage stability is reached and the capacitance measurement made. Capacitance measurements shall be made at each step specified in table XIII and at a sufficient number of intermediate points between step B and step G to establish a true characteristic curve. Capacitance measurements at each temperature shall be taken only after the test temperature has stabilized. For voltage ratings above 200 V, an approved alternate test method based on volts/mil stress of the same dielectric lot is allowed.

TABLE XIII. Voltage-temperature limit cycle.

Step 1/	Voltage, dc	Temperature, °C
A	None	+25 ± 2
B	None	-55 ± 2
C 2/	None	+25 ± 2
D	None	+125 +4, -0
E	Rated (see 3.1)	+125 +4, -0
F	Rated (see 3.1)	+25 ± 2
G	Rated (see 3.1)	-55 ± 2

1/ Step A through step D and step F (without voltage) only for BP and BG characteristics.
2/ Reference.

4.8.12 Thermal shock and immersion (see 3.15).

4.8.12.1 Thermal shock. Capacitors shall be tested in accordance with MIL-STD-202-107. The following details shall apply:

a. Test condition: Test condition A, except that in step 3, sample units shall be tested at +125°C.

b. Measurements before and after cycling: Not applicable.

4.8.12.2 Immersion. Following thermal shock, capacitors shall be tested in accordance with MIL-STD-202-104. The following details shall apply:

a. Test condition: Test condition B.

b. Examinations and measurements after final cycle: Capacitors shall meet the requirements of 3.15.

4.8.13 Resistance to soldering heat (see 3.16). Capacitors shall be tested in accordance with MIL-STD-202-210. The following details and exceptions shall apply:

a. Mounting of specimens: The capacitors shall be mounted on a substrate as specified in 4.8.1.

b. Test condition.

(1) Leaded capacitors: B.

(2) Nonleaded capacitors: J, except with only one heat cycle. The combination of the mounting process and 1 heat cycle is effectively equivalent to 2 heat cycles.

c. Measurements after test: After completion of the cleaning process and following a minimum 10-minute to maximum 24-hour cooling period, the capacitance, DF, and IR shall be measured as specified in 4.8.4, 4.8.5, and 4.8.6, respectively.

d. Examination after test: Capacitors shall be examined for evidence of mechanical damage.

4.8.14 Moisture resistance (see 3.17). Capacitors shall be tested in accordance with MIL-STD-202-106. The following details and exceptions shall apply:

a. Initial measurements: Capacitance as specified in 3.7.

b. Number of cycles: Twenty continuous cycles except that steps 7a and 7b shall be omitted.

c. Polarizing voltage shall be rated voltage (see 3.1) or 50 V_{dc}, whichever is less, during the first ten cycles.

d. Examinations and final measurements: On completion of step 6 of the final cycle, capacitors shall be conditioned at +25°C ± 5°C and a relative humidity between 30 percent and 60 percent for a period of 18 hours minimum to 24 hours maximum, and shall be visually examined for evidence of mechanical damage and obliteration of marking; capacitance, DWV, and IR shall then be measured as specified in 4.8.4, 4.8.9, and 4.8.6, respectively.

4.8.15 Humidity, steady state, low voltage (see 3.18). Capacitors shall be tested in accordance with MIL-STD-202-103, condition A. The following details and exceptions shall apply:

NOTE: At no time during test shall voltage greater than 1.55 volts be applied to any capacitor under test.

a. Conditioning: Not required.

b. Initial measurements: Capacitance shall be measured in accordance with 4.8.4.

c. Tests: Capacitors shall be subjected to an environment of +85°C with 85 percent relative humidity for 240 hours minimum. Cycling shall not be performed. A dc potential of 1.3 volts ± 0.25 volts shall be applied continuously through a 100 kilohm resistor.

d. Final measurements: On completion of test, remove the capacitors from the chamber and allow 3 hours, 30 minutes, ± 30 minutes for drying and stabilization at +25°C before performing IR (through a 100 kilohm resistor at 1.3 ± 0.25 volts) and capacitance in accordance with 4.8.6 and 4.8.4, respectively. The capacitors shall then be examined for evidence of mechanical damage and obliteration of marking.

e. Leads may be attached to chip capacitors for mounting and loading purposes. Mechanical loading is acceptable.

4.8.16 Life (at elevated ambient temperature)(see 3.19). Capacitors shall be tested in accordance with MIL-STD-202-108. The following details and exceptions shall apply:

a. Capacitors shall be mounted as specified in 4.8.1 and 4.8.1.1.

b. Test temperature and tolerance: At the maximum rated temperature, +125°C +4°C, -0°C.

c. Operating conditions: Capacitors shall be subjected to a minimum of 200 percent of rated voltage (see 3.1). The surge current shall not exceed 50 mA. When necessary, a suitable current-limiting resistor shall be inserted into the circuit.

d. Test condition: Test condition F (2,000 hours).

e. Measurements during and after exposure: After 1,000 hours and at the conclusion of this test and while the capacitors are still held at the maximum rated temperature, IR shall be measured as specified in 4.8.6. At the option of the manufacturer, the capacitors may be transferred to another chamber maintained at the same temperature for the purpose of measuring IR. The IR measurement shall be made only after the capacitors have stabilized at the test temperature. The capacitors shall then be returned to the inspection conditions specified in 4.3 and shall be visually examined for evidence of mechanical damage; capacitance, DF, and IR shall be measured as specified in 4.8.4, 4.8.5, and 4.8.6, respectively.

f. Final measurement: Capacitors shall meet the requirements of 3.19.

4.8.17 Series resonance (when specified, see 3.1)(see 3.20). Capacitors shall be mounted as specified in 4.8.1 and tested to determine minimum series resonance frequency. Measurement frequency shall be varied smoothly between 100 MHz and 10,000 MHz.

4.8.18 Terminal integrity (see 3.21).

4.8.18.1 Nonleaded capacitors.

4.8.18.1.1 Board flex test (see 3.21.1.1). Capacitors shall be tested ~~for board flex~~ in accordance with MIL-STD-202-218. ~~t~~The following details and exceptions shall apply:

a. Mounting: In accordance with MIL-STD-202-218. ~~Capacitors shall be mounted in accordance with 4.8.1 on a 3.94 inches (100 mm) ± .079 inch (2.0 mm) X 1.57 inches (40 mm) ± .079 inch (2.0 mm) FR4 printed circuit board (PCB), which is .063 inch (1.6 mm) ± .008 inch (0.20 mm) thick.~~At the option of the manufacturer, the length and width of the PCB may be increased to allow for electrical test connections and multiple samples to be mounted and subjected to the board flex test. Testing and all other dimensions shall remain as specified.

b. Procedure: The FR4 PCB shall be placed into a fixture similar to the one shown in figure 3 with the component facing down. A force shall be applied which will bend the board .079 inch (2.0 mm), minimum.

At the option of the manufacturer, the configuration of the PCB and fixture may be vertical or horizontal provided the force applied is in the direction specified in figure 3.

c. Duration of force: The duration of the applied force shall be 60 seconds -0, + 5 seconds.

d. Measurement during test: Capacitance as specified in 4.8.4.

ce. Examinations and measurements after test: Capacitors shall be visually inspected for mechanical damage to the device capacitor body, terminals, and body/terminal junction. Capacitance and dissipation factor shall then be measured as specified in 4.8.4 and 4.8.5.

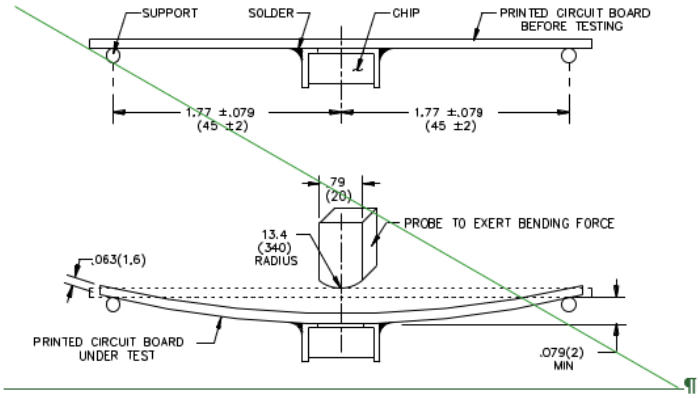


FIGURE 3. Board flex.

4.8.18.1.2 Shear stress test (see 3.21.1.2). Capacitors shall be tested for shear stress in accordance with MIL-STD-202-219.the following:

a. Mounting: Capacitors shall be mounted as specified in 4.8.1.

b. Procedure: The specified force shall be applied to the side of the capacitor being tested (see figure 4). The applied force shall be parallel with the plane of the test board and perpendicular to the side of the capacitor. The force shall be applied gradually as not to apply a shock to the capacitor.

c. Duration of force: The force shall be applied for 60 seconds ±1 second.

d. Magnitude of force applied:

Part Size	Force (Kg)
> 1210	1.8
≥ 0603 and ≤ 1210	1.0
0402	0.5

e. Examination after test: Capacitors shall be visually inspected for mechanical damage to the device body, terminals, and body/terminal junction.

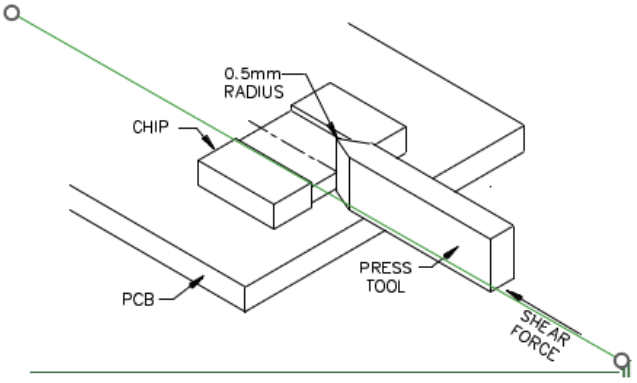


FIGURE 4. Shear stress.

4.8.18.2 Leaded capacitors.

4.8.18.2.1 Terminal strength (see 3.21.2.1). Capacitors shall be tested in accordance with MIL-STD-202-211. The following details and exceptions shall apply:

a. Test condition: B (five bends).

b. Examination after test: Visual examination for loosening, rupturing, and permanent damage to the terminals.

4.8.19 Temperature coefficient and capacitance drift (high frequency capacitors only) (see 3.22).

4.8.19.1 Temperature coefficient. Capacitance measurements shall be made as specified in 4.8.4 and at the temperatures specified in table XIII.

4.8.19.2 Capacitance drift. Capacitance drift shall be computed by dividing the greatest single difference between any two of the three capacitance values recorded at +25°C by the value determined at the reference temperature (see table XIII).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the military service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Ceramic chip capacitors are intended to be used in thin and thick film hybrid circuits where micro-circuitry is indicated for filter by-pass coupling applications, and where variation in capacitance with respect to temperature (-55°C to +125°C), voltage, frequency, and life can be tolerated. This specification also covers high frequency capacitors (CDR11 through CDR14 and CDR21 through CDR25) that are primarily intended for use in resonant circuits with high Q factor and stability of capacitance with respect to temperature (-55°C to +125°C), frequency, and life. These capacitors also offer established reliability that is verified under a qualification system. Commercial components are not designed to withstand these military environmental conditions.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification, the applicable specification sheet, and the complete PIN (see 1.2.1 and 3.1).

b. Capacitor marking (see 3.23).

c. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products that are, at the time of award of contract, qualified for inclusion in the Qualified Products List whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. ~~The activity responsible for the Qualified Products List is CERDEC PRD: RDER-PRO, Building 6010 K-130, Aberdeen Proving Ground, Aberdeen, MD 21005; however, i~~Information pertaining to qualification of products may be obtained from the DLA Land and Maritime, ATTN: VQP, PO Box 3990, Columbus, OH 43218-3990, or by e-mail to vqp.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 Metallized terminations. It should be noted that when pure silver is used for the termination, silver migration between the terminations may occur under conditions of simultaneous application of high humidity and dc voltage. This produces a troublesome electrical leakage path across the capacitor chip. Addition of about 20 percent of palladium to the silver to form an alloy will retard the tendency toward silver migration. Complete overcoating of the silver termination by the lead-tin bonding solder also will retard the tendency toward silver migration. Addition of about 3 percent of silver to the lead-tin bonding solder will tend to reduce the leaching of silver from the silver termination during the solder bonding operation.

6.4.1 Termination finish N. Solder embrittlement may take place if termination finish N is used with tin-lead solder.

6.4.2 Tin whisker growth. The use of alloys with tin content greater than 97 percent, by mass, may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture and can develop under typical operating conditions, on products that use such materials. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys of 3 percent lead, by mass, have shown to inhibit the growth of tin whiskers. For additional information on this matter, refer to ASTM-B545 (Standard Specification for Electrodeposited Coatings of Tin).

6.5 Wave soldering. Chips larger than 1206 are not recommended for wave soldering. Wave soldering uses liquid metal that has the highest heat transfer rate and is the hardest soldering method to use without shocking surface mount components. When extreme thermal shock is present, it is very obvious with visible cracks on the surface and sides of the capacitor. These cracks start at or near the termination and ceramic interface extending from the termination down along the capacitor edge. These surface cracks can become elliptical or circular shaped in the larger capacitor sizes. The cracks can eventually lead to failure of the capacitors. Some of this information was taken from MIL-PRF-55681 manufacturer's internet sites. The manufacturers should be contacted for further information.

6.6 Ambient operating conditions. Designers are cautioned to give consideration to the change in dielectric constant with temperature, shelf aging, and electric-field intensity, and should recognize that the IR may vary with humidity and organic contamination of the ceramic chip surfaces. Care should be taken to assure that the capacitors are properly and thoroughly cleansed of organic contamination, especially before the IR test.

6.7 Barometric pressure test. These units are not subject to the barometric pressure test since the likelihood of their failure is remote.

6.8 Effect of mounting on reliability. Voltage-temperature limits and resistance to thermal shock, and reliability may be affected as a result of mounting on substrate with dissimilar coefficients of expansion from capacitor material. Care should be taken in the selection of substrate material.

6.9 Supersession data. Capacitors of this specification are not intended to be used for replacement purposes. Therefore, no interchangeability and substitution data are offered.

6.10 Selection and use information. Equipment designers should refer to MIL-HDBK-198, "Capacitors, Selection and Use of", for a selection of standard capacitor types and values for new equipment design. Additional application and use information concerning these capacitors is also provided in MIL-HDBK-198.

6.11 Supplying for logistic support. Chip components require use of sophisticated equipment to remove from and install on printed wiring boards. Only requisitioners with in-house or contracted capability to replace surface mounted components should be supplied with chip components, in accordance with their specification.

6.12 Nickel electrodes. Performance requirements for ceramic chip capacitors manufactured with nickel electrodes may be found in MIL-PRF-32535 (Capacitor, Chip, Fixed, Ceramic Dielectric (Temperature Stable and General Purpose), Extended Range, High Reliability and Standard Reliability, General Specification for).

6.13 Subject term (key word) listing.

Part per million (ppm)
Statistical process control (SPC)

6.14 Intended assembly methods for surface mount capacitors. The intended assembly methods for surface mount ceramic capacitors depend on the capacitor's termination style as shown by "Type" in table IV. The use of assembly methods other than those intended for each termination style may result in reduced performance (e.g., potential for gold embrittlement of tin-lead solder joints if soldering to gold-finished components). Where noted in this specification (see 4.8.16, 4.8.18.1.1, and 4.8.18.1.2), certain tests that require assembly of the surface mount capacitors to test cards may require or give the manufacturer the option to use assembly methods other than those intended for the termination style being tested (e.g., for life test (4.8.16) the manufacturer is required to solder assemble gold-finished capacitors).

6.15 Changes from previous issue. The margins of this specification are marked with vertical lines to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.~~Amendment notations. The margins of this specification are marked with vertical lines to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.~~

EQUIVALENT SERIES RESISTANCE MEASUREMENT CRITERIA FOR HIGH FREQUENCY CAPACITOR STYLES CDR11 THROUGH CDR14 AND CDR21 THROUGH CDR25

A.1 SCOPE

A.1.1 Scope. This appendix specifies the method to determine high frequency loss as measured by equivalent series resistance (ESR). This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS

A.2.1 General. The documents listed in this section are specified in this appendix. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of the documents cited in this appendix, whether or not they are listed.

A.2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ELECTRONIC COMPONENTS INDUSTRY ASSOCIATION (ECIA)

~~ECIA-483~~ECIA RS-483 -	Standard Method of Test for Effective Series Resistance (ESR) and Capacitance of Multilayer Ceramic Capacitors at High Frequencies

(Copies of these documents are available from ~~http://www.ecianow.org~~https://www.ecianow.org/.)

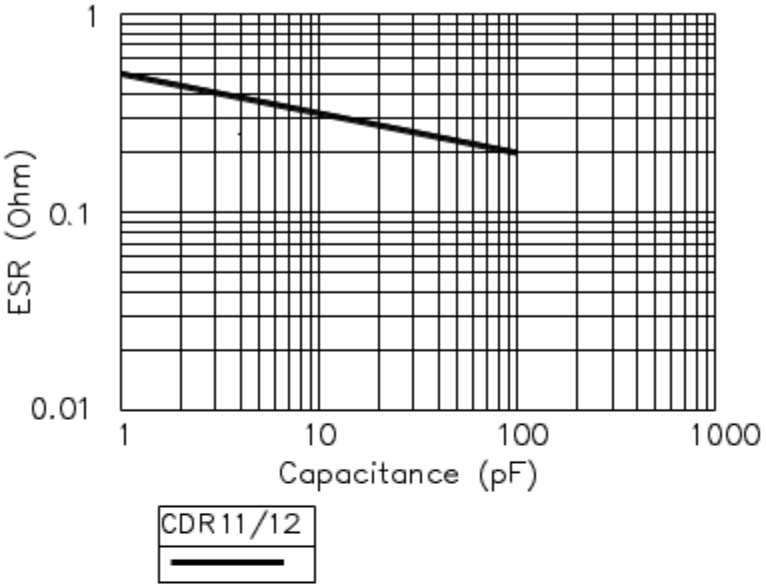
A.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 PROCEDURES FOR TEST

A.3.1 ESR. When specified, the ESR shall be measured in accordance with ~~ECIA-483~~ECIA RS-483.

A.4 TEST CRITERIA

A.4.1 ESR. When ESR is tested in accordance with A.3.1, ESR shall be less than the limits shown on figure A-1 through figure A-4 at the specified measurement frequency range.



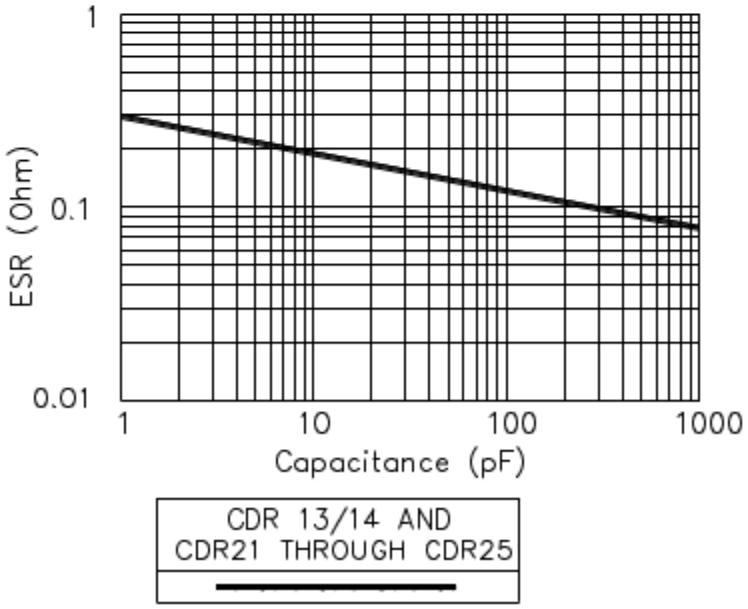


FIGURE A-1. ESR (UHF) (BG characteristic).

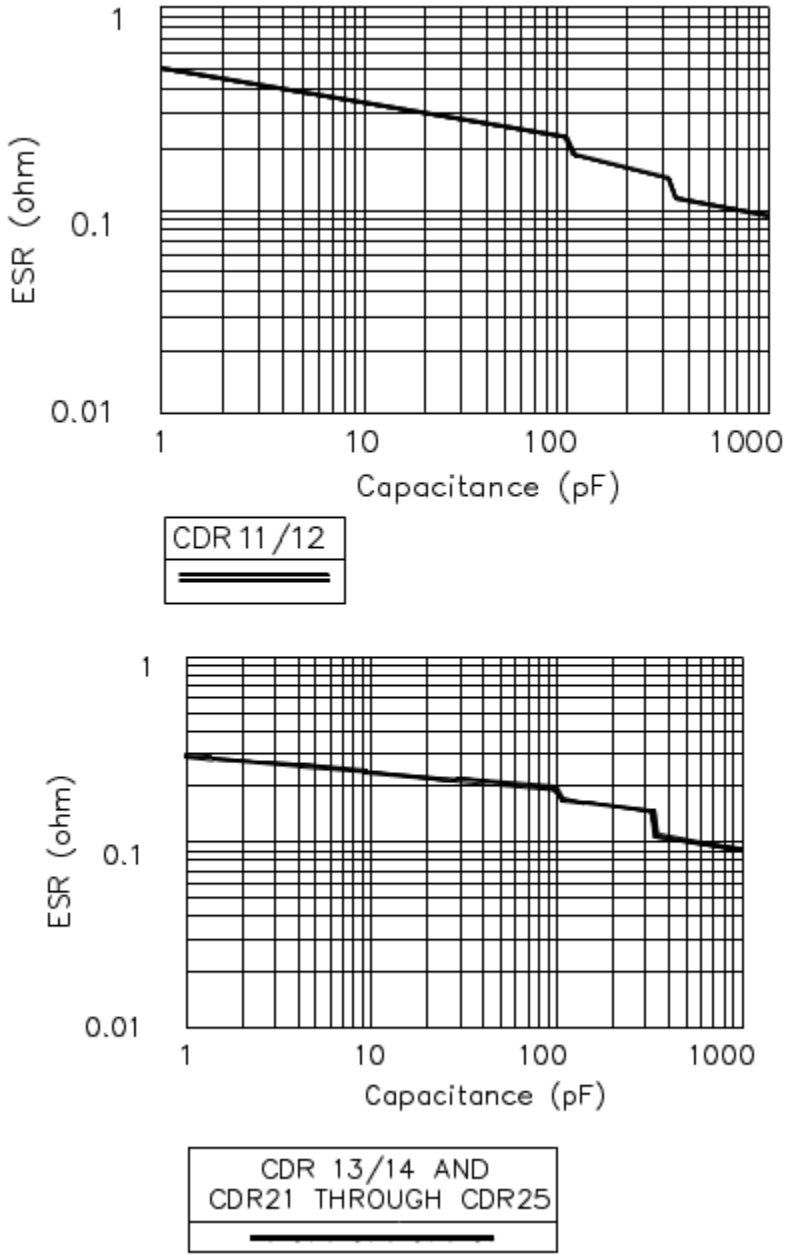


FIGURE A-2. ESR (UHF) (BP characteristic).

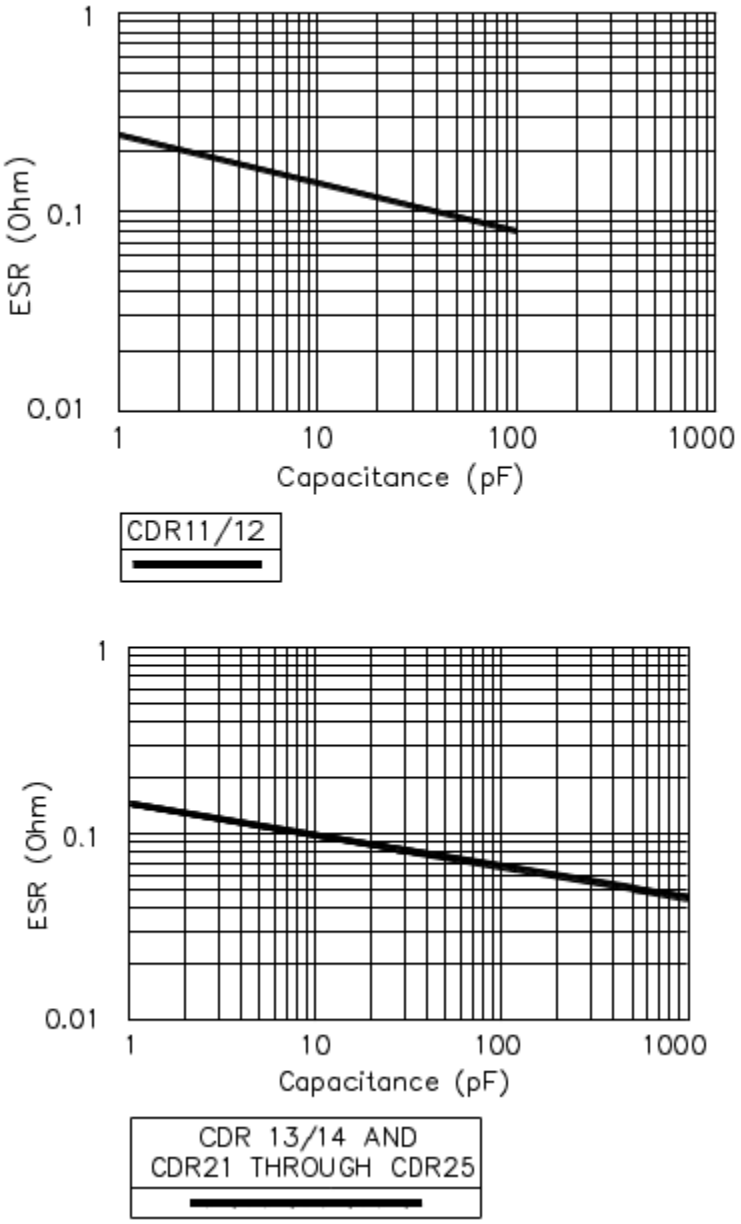


FIGURE A-3. ESR (RF) (BG characteristic).

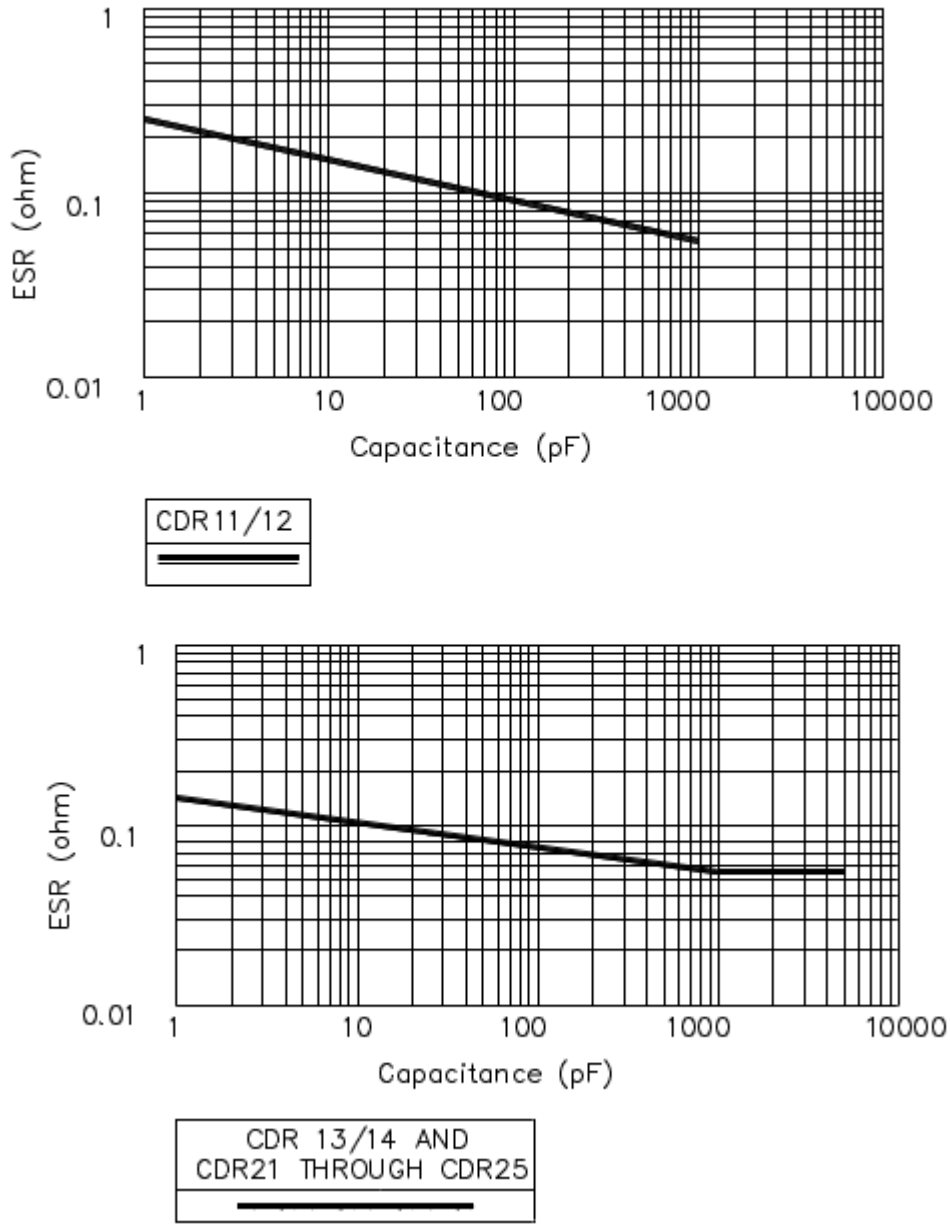


FIGURE A-4. Equivalent series resistance (RF) (BP characteristic)

PROCEDURE FOR QUALIFICATION INSPECTION

B.1 SCOPE

B.1.1 Scope. This appendix details the procedure for submission of samples for qualification inspection of capacitors covered by this specification. The procedure for extending qualification of the required sample to other capacitors covered by this specification is also outlined herein. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

B.2 SUBMISSION

B.2.1 Sample.

B.2.1.1 Single-style submission. A sample consisting of 97 sample units of the highest capacitance value in each voltage rating, in each rated temperature and voltage-temperature limits, in each style for which qualification is sought shall be submitted. After qualification has been granted, no changes shall be made in materials, design, or construction without prior notification of the qualifying activity.

B.2.1.2 Combined-voltage submission. A sample consisting of sample units of the highest capacitance value in each voltage rating, in each rated temperature and voltage-temperature limits, in each style for which qualification is sought shall be submitted (see table B-I). After qualification has been granted, no changes shall be made in materials, design, or construction without prior notification of the qualifying activity.

B.3 EXTENT OF QUALIFICATION

B.3.1 Single-style submission. Capacitance-range qualification will be restricted to values equal to and less than the capacitance value submitted. Voltage rating qualification will be restricted to that submitted. Qualification may be extended to lower voltages than that submitted if the manufacturer can demonstrate that the capacitor design is the same. Rated temperature and voltage-temperature limit qualification will be restricted to that submitted.

B.3.2 Combined-voltage submission (see table B-I). Capacitance-range qualification will be restricted to values equal to and less than the capacitance value submitted. Voltage rating qualification will be restricted to those submitted. Qualification may be extended to lower voltages than that submitted if the manufacturer can demonstrate that the capacitor design is the same.

B.3.3 Termination finish. For initial qualifications, ~~T~~termination finish qualification will be restricted to that submitted (see table IV). Additional termination finishes may be qualified by performing the following tests (as applicable) in accordance with table VIII (qualification inspection): Solderability, resistance to soldering heat, life (at elevated ambient temperature), board flex, and shear stress. Termination qualification due to expansions of current offerings or process changes shall be determined by the qualifying activity. ~~Qualification of a termination finish on a single style will extend to all styles for which qualification is sought.~~

B.3.4 Product levels. Qualification of the C (non-ER) level is predicated upon meeting the qualification requirements for ER FRL "P". Since the non-ER (C level) is the ER design without the mandatory conformance inspection and FRL assessment, this product is still expected to meet the environmental requirements (e.g., moisture resistance, thermal shock, shock, etc).

B.3.5 Metric styles. Qualification of metric styles CDR31, CDR34, and CDR35 will extend qualification to styles CDR01, CDR04, and CDR05 respectively. Capacitance range, voltage rating, and rated temperature and voltage-temperature limit qualification will be restricted as specified in B.3.1.

B.3.6 Extension of failure rate level qualification of CDR36 and CDR37 styles. Upon the successful completion of the initial qualification inspection (see table VIII) of CDR36 and CDR37 styles, manufacturers that are currently qualified to the CDR31 (/7) style to a specific failure rate level are eligible for CDR36 and CDR37 qualification to the same failure rate level by similarity.

TABLE B-I. Combined-voltage submission. 4/

Style	PIN 3/	Number of units 1/	Rated voltage
CDR01	BP181B - - M BX332B - - M BX472A - - M	97 2/ 49 2/ 49	100 100 50
CDR02	BP271B - - M BX103B - - M BX223A - - M	97 2/ 49 2/ 49	100 100 50
CDR03	BP102B - - M BX333B - - M BX683A - - M	97 2/ 49 2/ 49	100 100 50
CDR04	BP332B - - M BX563B - - M BX184A - - M	97 2/ 49 2/ 49	100 100 50
CDR05	BP562B - - M BX154B - - M BX334A - - M	97 2/ 49 2/ 49	100 100 50
CDR06	BP103B - - M BX474A - - M	97 97	100 50
CDR11 and CDR12	B -101K - - M BP102B - - M BP102A - - M	49 49 49	150 100 50
CDR13 and CDR14	B -101E - - M B -201D - - M B -471C - - M B -621B - - M B -102A - - M BP512A - - M	97 2/ 49 2/ 49 2/ 49 2/ 49 2/ 49	500 300 200 100 50 50
CDR21 and CDR22	B -101E - TM B -201D - TM B -471C - TM B -621B - TM B -102A - TM BP512A - TM	97 2/ 49 2/ 49 2/ 49 2/ 49 2/ 49	500 300 200 100 50 50
CDR23 and CDR24	B -101E - - M B -201D - - M B -471C - - M B -621B - - M B -102A - - M BP512A - - M	97 2/ 49 2/ 49 2/ 49 2/ 49 2/ 49	500 300 200 100 50 50
CDR25	B -101E - SM B -201D - SM B -471C - SM B -621B - SM B -102A - SM BP512A - SM	97 2/ 49 2/ 49 2/ 49 2/ 49 2/ 49	500 300 200 100 50 50
CDR31	BP471B - - M BP681A - - M BX472B - - M BX183A - - M	49 49 49 49	100 50 100 50

See footnotes at end of table.

TABLE B-I. Combined-voltage submission - Continued. 4/

Style	PIN 3/	Number of units 1/	Rated voltage
CDR32	BP102B - - M	49	100
	BP222A - - M	49	50
	BX153B - - M	49	100
	BX393A - - M	49	50
CDR33	BP222B - - M	49	100
	BP332A - - M	49	50
	BX273B - - M	49	100
	BX104A - - M	49	50
CDR34	BP472B - - M	49	100
	BP103A - - M	49	50
	BX563B - - M	49	100
	BX184A - - M	49	50
CDR35	BP103B - - M	49	100
	BP223A - - M	49	50
	BX154B - - M	49	100
	BX474A - - M	49	50
CDR36	BP331B - - M	25	100
	BP102A - - M	25	50
	BP152Z - - M	25	25
	BP152Y - - M	25	16
	BX272B - - M	25	100
	BX103A - - M	25	50
	BX273Z - - M	25	25
	BX104Y - - M	25	16
	BR102C - - M	25	200
	BR822B - - M	25	100
	BR273A - - M	25	50
	BR563Z - - M	25	25
	BR104Y - - M	25	16
CDR37	BP181B - - M	25	100
	BP221A - - M	25	50
	BP221Z - - M	25	25
	BP331Y - - M	25	16
	BX681B - - M	25	100
	BX182A - - M	25	50
	BX392Z - - M	25	25
	BX822Y - - M	25	16
	BR102B - - M	25	100
	BR392A - - M	25	50
	BR472Z - - M	25	25
	BR103Y - - M	25	16

1/ The number of units shown shall be submitted for each termination finish.
2/ Table VIII, group V samples may be split 12-13 or 13-12.
3/ The complete PIN will include additional symbols to indicate rated temperature and voltage-temperature limits (where applicable), capacitance tolerance, and termination finish (where applicable) (see 1.2.1).
4/ This table is set up as a guide. Other combinations may be considered; however, the total number of units in each voltage-temperature limit shall be 97, minimum.

VISUAL INSPECTION CRITERIA

C.1 SCOPE

C.1.1 Scope. This appendix specifies the visual inspection criteria. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

C.2 PROCEDURES FOR INSPECTION AND REJECTION

C.2.1 Method of inspection. Each device shall be examined under 20X to 40X magnification to determine compliance with the requirements specified herein.

C.2.2 Rejection criteria. Devices that deviate from the material, design or construction requirements specified, or that fail to meet the following requirements, shall be unacceptable.

C.2.2.1 Termination metallization.

a. End terminals shall be completely covered. For chip sizes 0805 and larger, pinholes less than or equal to .005 inch (0.13 mm) in diameter are permitted (maximum of three pinholes in each surface area). For chip sizes smaller than 0805, pinholes less than or equal to .003 inch (0.08 mm) in diameter are permitted (maximum of three pinholes in each surface area).

b. Gaps in the metallization band shall only be acceptable if the metallization band is not less than the minimum metallization band requirement specified (see figure C-1).

c. Metallized edges shall not be reduced to less than 90 percent due to chipping or metallizing process (see figure C-2).

d. There shall be no excess metallization or solder tear which violates the minimum pad separation (see figure C-3).

e. There shall be no foreign material visible adhering to the solder, or voids in the solder revealing greater than 10 percent of the base metallization (see figure C-4).

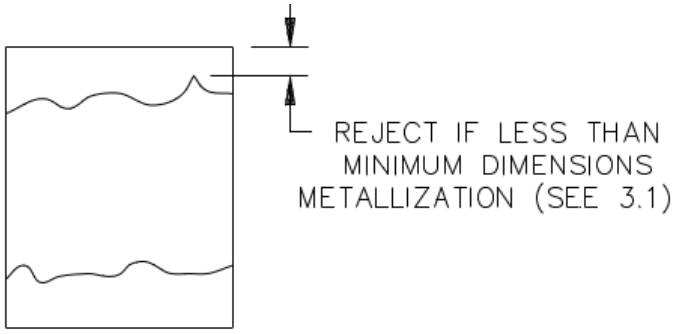


FIGURE C-1. Metallization band gaps.

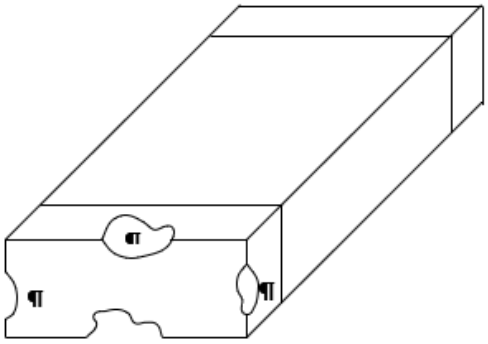


FIGURE C-2. Metallization band chipping.

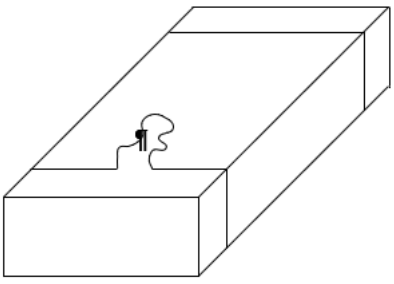


FIGURE C-3. Excessive metallization.

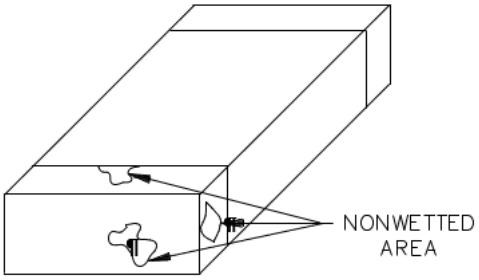


FIGURE C-4. Solder defects.

C.2.2.2 Ceramic surface examination.

a. There shall be no cracks (see figure C-5). A crack is a very slight separation along or across a boundary that usually occurs after sintering.

b. There shall be no delamination of ceramic layers. A delamination is the separation of ceramic layers (usually observed on sides). (see figure C-6.)

c. Striations are unacceptable (see figure C-6). Striations are vitrified layers without any actual separation.

d. Chip-outs or chip-ins shall not extend under the end terminations or expose electrode plates. A chip-out is an area where ceramic has broken free from the capacitor (see figure C-7). A chip-in is an area where ceramic can be seen to be forming a chip-out; however, the ceramic is still intact.

e. Rough edges shall be permitted provided they are within the allowable chip-out region as specified in figure C-7.

f. Lips, flared edges, or irregular shapes shall not exceed the specified dimensional limits (see 3.1 and figure C-8).

g. There shall be no fused dust or excess material on external surface that prevents a chip from lying flat, or protrude more than .003 inch (0.08 mm) out of a surface.

h. There shall be no raised surfaces, bubbles, or blisters greater than .002 inch (0.05 mm) (usually found on top and bottom) (see figure C-9).

i. When compared to a flat surface, the clearance (warpage) at the center of the chip shall be less than 5 percent of the length dimension (see figure C-10).

j. There shall be no pinholes larger than .002 inch (0.05 mm) in diameter (see figure C-11). A pinhole is a circular hollow or cavity.

k. There shall be no holes (voids) that expose electrode plates (see figure C-12).

l. The marking (when specified) shall be legible and complete (see figure C-13).

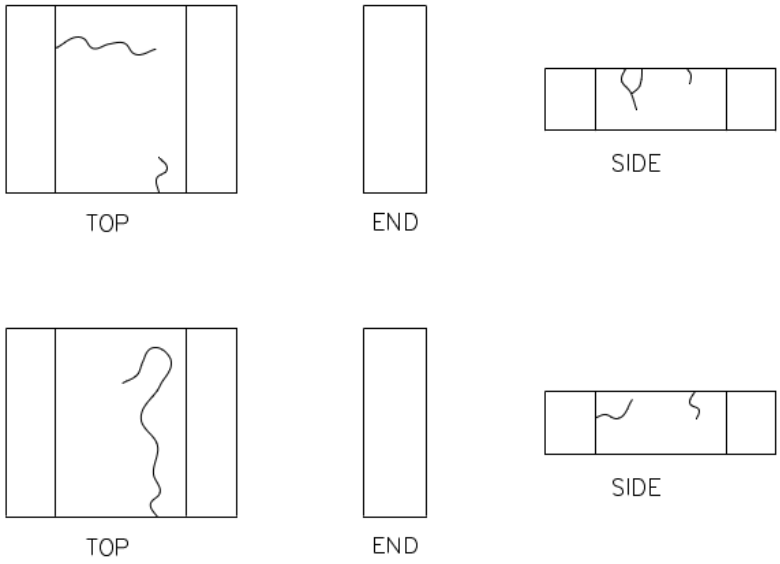


FIGURE C-5. Cracks.

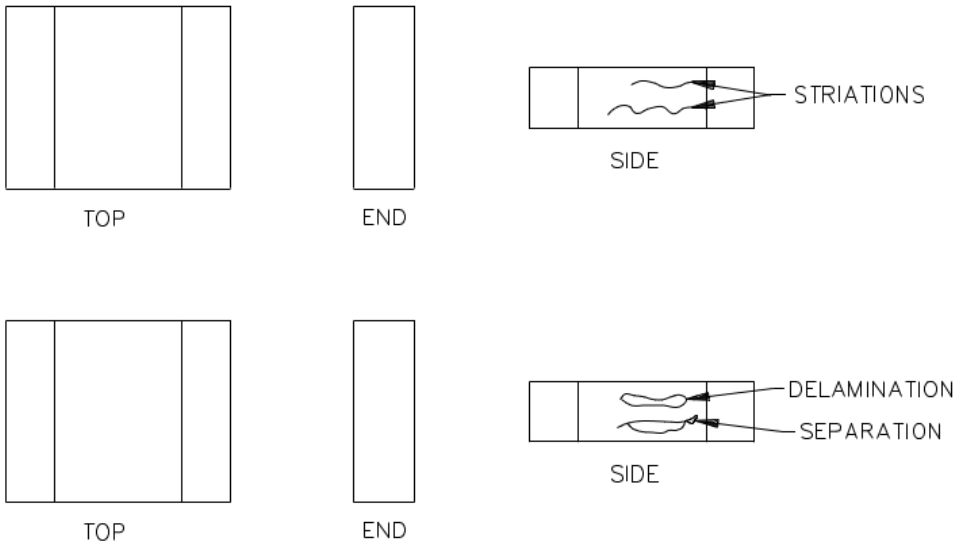


FIGURE C-6. Striations and delaminations.

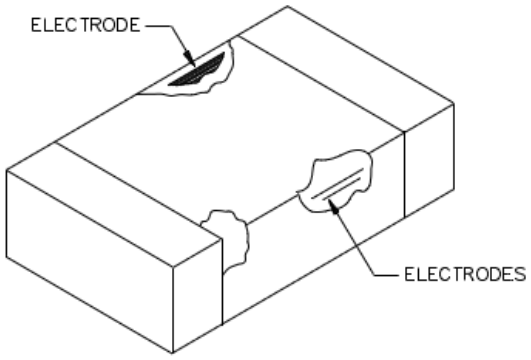


FIGURE C-7. Chip-outs and chip-ins.

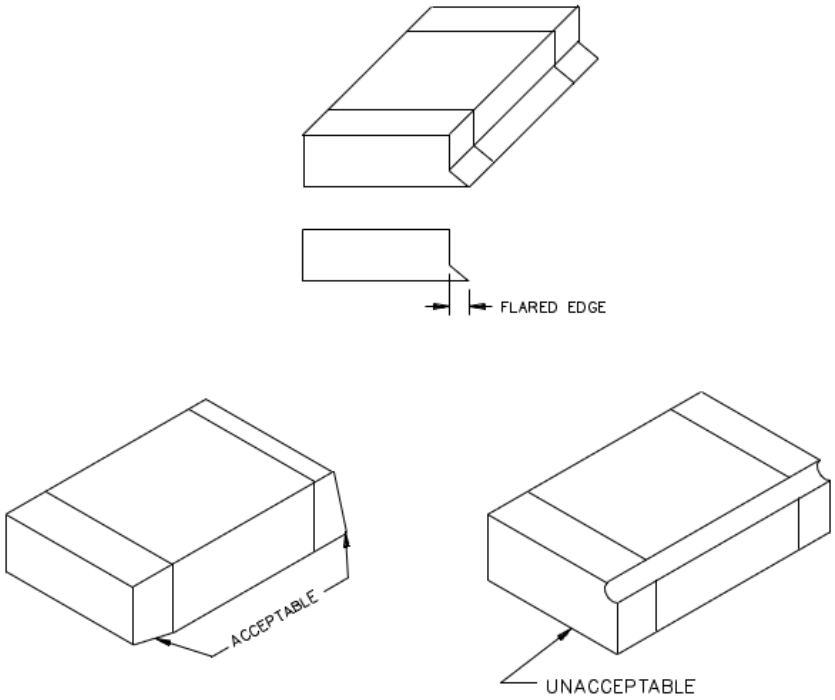


FIGURE C-8. Unacceptable lips, flared edges, or irregular shapes.

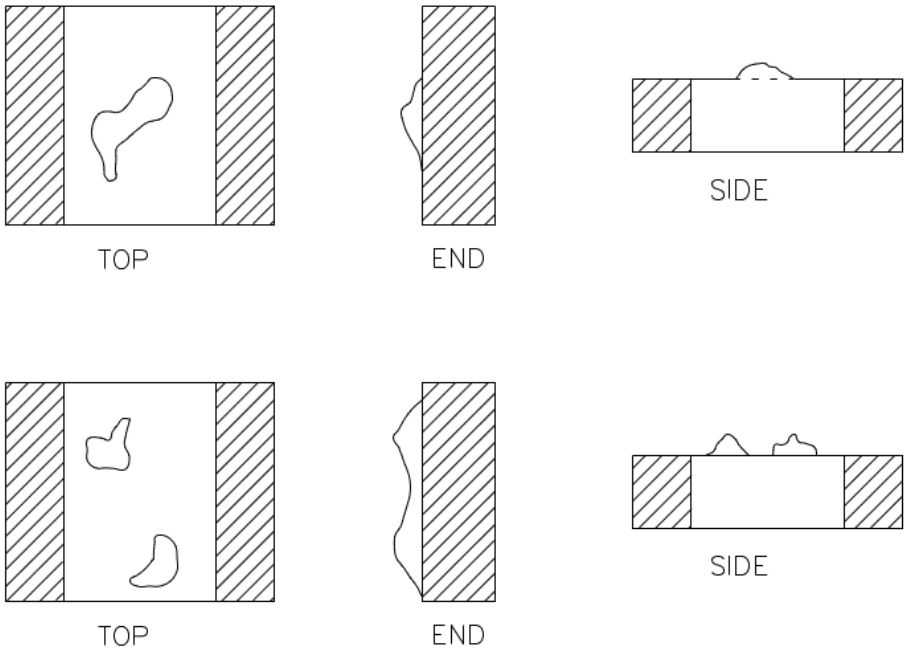


FIGURE C-9. Raised surfaces, bubbles, and blisters.

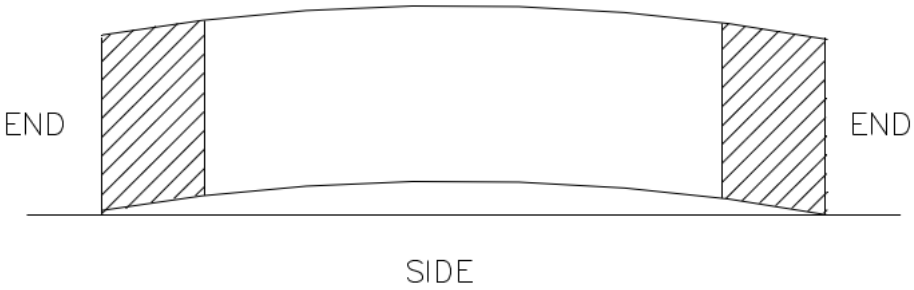


FIGURE C-10. Warpage.

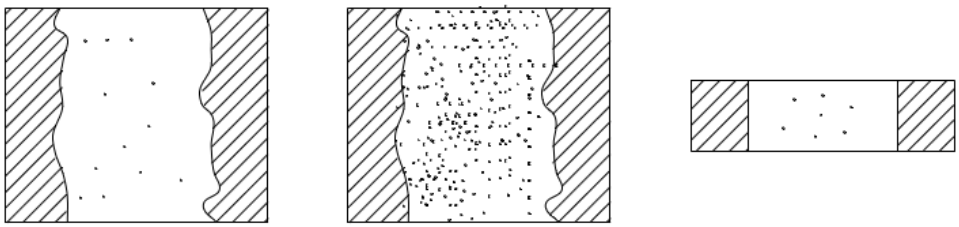


FIGURE C-11. Pinholes.

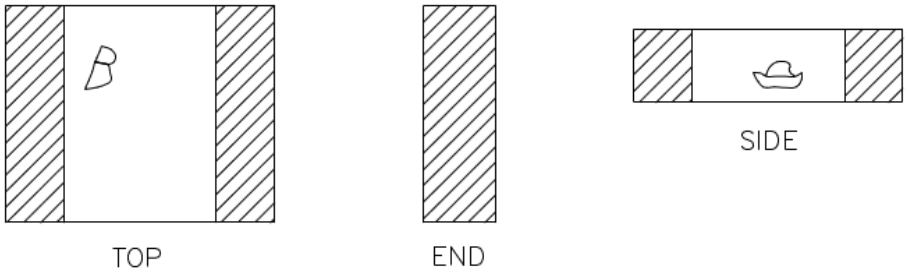


FIGURE C-12. Voids.

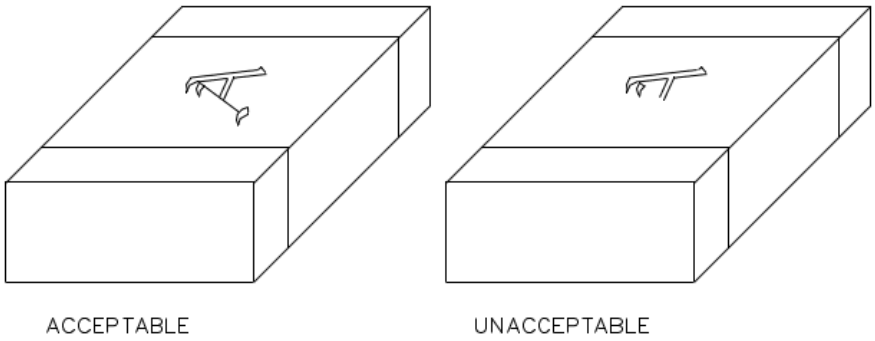


FIGURE C-13. Marking.

Custodians:
Army - CR
Navy - EC
Air Force - 85
DLA - CC

Preparing activity:
DLA - CCArmy - CR

(Project 5910-2025-00817 039)Agent:
DLA - CC

Review activities:
Army - MI
Navy - AS, MC, OS, SH
Air Force - 19, 99
Other DoD - MDA

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using ASSIST Online database at https://assist.dla.mil.

NOTE: This draft, dated 14 January 2025, prepared by DLA-CC, has not been approved and is subject to modification.
DO NOT USE PRIOR TO APPROVAL. (Project 5910-2025-008S)

INCH-POUND
MIL-PRF-55681H~~G~~
SUPPLEMENT 1
~~12 July 2016~~DRAFT

PERFORMANCE SPECIFICATION

CAPACITOR, CHIP, MULTIPLE LAYER, FIXED,
CERAMIC DIELECTRIC, ESTABLISHED RELIABILITY
AND NON-ESTABLISHED RELIABILITY,
GENERAL SPECIFICATION FOR

This supplement forms a part of MIL-PRF-55681H~~G~~, dated DD Month YYYY~~12 July 2016~~.

SPECIFICATION SHEETS

MIL-PRF-55681/1	-	Capacitors, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, Styles CDR01, CDR02, CDR03, and CDR04
MIL-PRF-55681/2	-	Capacitors, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, Style CDR05
MIL-PRF-55681/3	-	Capacitors, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, Style CDR06
MIL-PRF-55681/4	-	Capacitor, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, Styles CDR11, CDR12, CDR13, and CDR14 (High Frequency)
MIL-PRF-55681/5	-	Capacitors, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, Styles CDR21, CDR22, CDR23, CDR24, and CDR25 (High Frequency)
MIL-PRF-55681/7	-	Capacitors, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, Style CDR31, Metric
MIL-PRF-55681/8	-	Capacitors, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, Style CDR32, Metric
MIL-PRF-55681/9	-	Capacitors, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, Style CDR33, Metric
MIL-PRF-55681/10	-	Capacitors, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, Style CDR34, Metric
MIL-PRF-55681/11	-	Capacitors, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, Style CDR35, Metric
MIL-PRF-55681/12	-	Capacitor, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, Style CDR36
MIL-PRF-55681/13	-	Capacitor, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, Style CDR37

TABLE I. Available values.

Specification sheet	Style	Chip size	Dielectric	Voltage (V_{dc})	Values	Notes
1	CDR01	0805	BP	100	10pF - 180pF	
1	CDR01	0805	BX	100	120pF - 3,300pF	
1	CDR01	0805	BX	50	3,900pF - 4,700pF	
1	CDR02	1805	BP	100	220pF - 270pF	
1	CDR02	1805	BX	100	3,900pF - 10,000pF	
1	CDR02	1805	BX	50	12,000pF - 22,000pF	
1	CDR03	1808	BP	100	330pF - 1,000pF	
1	CDR03	1808	BX	100	12,000pF - 33,000pF	
1	CDR03	1808	BX	50	39,000pF - 68,000pF	
1	CDR04	1812	BP	100	1,200pF - 3,300pF	
1	CDR04	1812	BX	100	39,000pF - 56,000pF	
1	CDR04	1812	BX	50	82,000pF - 180,000pF	
2	CDR05	1825	BP	100	3,900pF - 5,600pF	
2	CDR05	1825	BX	100	68,000pF - 150,000pF	
2	CDR05	1825	BX	50	220,000pF - 330,000pF	
3	CDR06	2225	BP	100	6,800pF - 10,000pF	
3	CDR06	2225	BX	50	390,000pF - 470,000pF	
4	CDR11, CDR12	0505	BG, BP	50, 150	.1pF - 100pF	High frequency
4	CDR11, CDR12	0505	BP	50, 100	110pF - 1,000pF	High frequency
4	CDR13, CDR14	1111	BG, BP	200, 500	.1pF - 100pF	High frequency
4	CDR13, CDR14	1111	BG, BP	200, 300	110pF - 200pF	High frequency
4	CDR13, CDR14	1111	BG, BP	200	220pF - 470pF	High frequency
4	CDR13, CDR14	1111	BG, BP	100	510pF - 620pF	High frequency
4	CDR13, CDR14	1111	BG, BP	50	680pF - 1,000pF	High frequency
4	CDR13, CDR14	1111	BP	50	1,100pF - 5,100pF	High frequency
5	CDR21 thru CDR25	1311	BG, BP	500	.1pF - 100pF	High frequency, leaded
5	CDR21 thru CDR25	1311	BG, BP	300	110pF - 200pF	High frequency, leaded
5	CDR21 thru CDR25	1311	BG, BP	200	220pF - 470pF	High frequency, leaded
5	CDR21 thru CDR25	1311	BG, BP	100	510pF - 620pF	High frequency, leaded
5	CDR21 thru CDR25	1311	BG, BP	50	680pF - 1,000pF	High frequency, leaded
5	CDR21 thru CDR25	1311	BP	50	1,100pF - 5,100pF	High frequency, leaded
7	CDR31	0805	BP	100	1pF - 470pF	
7	CDR31	0805	BP	50	510pF - 680pF	
7	CDR31	0805	BX	100	470pF - 4700pF	
7	CDR31	0805	BX	50	5,600pF - 18,000pF	
8	CDR32	1206	BP	100	1pF - 1,000pF	
8	CDR32	1206	BP	50	1,100pF - 2,200pF	
8	CDR32	1206	BX	100	4,700pF - 15,000pF	
8	CDR32	1206	BX	50	18,000pF - 39,000pF	
9	CDR33	1210	BP	100	1,000pF - 2,200pF	
9	CDR33	1210	BP	50	2,400pF - 3,300pF	
9	CDR33	1210	BX	100	15,000pF - 27,000pF	
9	CDR33	1210	BX	50	39,000pF - 100,000pF	
10	CDR34	1812	BP	100	2,200pF - 4,700pF	
10	CDR34	1812	BP	50	5,100pF - 10,000pF	
10	CDR34	1812	BX	100	27,000pF - 56,000pF	
10	CDR34	1812	BX	50	100,000pF - 180,000pF	
11	CDR35	1825	BP	100	4,700pF - 10,000pF	
11	CDR35	1825	BP	50	11,000pF - 22,000pF	
11	CDR35	1825	BX	100	56,000pF - 150,000pF	
11	CDR35	1825	BX	50	180,000pF - 470,000pF	

TABLE I. Available values - continued.

Specification sheet	Style	Chip size	Dielectric	Voltage (V_{dc})	Values	Notes
12	CDR36	0603	BP	100 1/	.5pF – 330pF	
12	CDR36	0603	BP	50 1/	390pF – 1,000pF	
12	CDR36	0603	BP	25 1/	1,200pF – 1,500pF	
12	CDR36	0603	BX	100 1/	100pF – 2,700pF	
12	CDR36	0603	BX	50 1/	3,300pF – 10,000pF	
12	CDR36	0603	BX	25 1/	12,000pF – 27,000pF	
12	CDR36	0603	BX	16 1/	33,000pF – 100,000pF	
12	CDR36	0603	BR	200 1/	100pF – 1,000pF	
12	CDR36	0603	BR	100 1/	1,200pF – 8,200pF	
12	CDR36	0603	BR	50 1/	10,000pF – 27,000pF	
12	CDR36	0603	BR	25 1/	33,000pF – 56,000pF	
12	CDR36	0603	BR	16 1/	68,000pF – 100,000pF	
13	CDR37	0402	BP	100 1/	.5pF – 180pF	
13	CDR37	0402	BP	50 1/	220pF	
13	CDR37	0402	BP	16 1/	270pF – 330pF	
13	CDR37	0402	BX	100 1/	100pF – 680pF	
13	CDR37	0402	BX	50 1/	820pF – 1,800pF	
13	CDR37	0402	BX	25 1/	2,200pF – 3,900pF	
13	CDR37	0402	BX	16 1/	4,700pF – 8,200pF	
13	CDR37	0402	BR	100 1/	100pF – 1,000pF	
13	CDR37	0402	BR	50 1/	1,200pF – 3,900pF	
13	CDR37	0402	BR	25 1/	4,700pF	
13	CDR37	0402	BR	16 1/	5,600pF – 10,000pF	

1/ This is the maximum rated voltage available. All lower voltage ratings are also available (In V_{dc}: V = 4, W = 6.3, X = 10, Y = 16, Z = 25, A = 50, B = 100, and C = 200).

Custodians:
Army - CR
Navy - EC
Air Force - 85
DLA - CC

Preparing activity:
DLA - CCArmy - CR

Agent:
DLA - CC

Review activities:
Army - MI
Navy - AS, MC, OS, SH
Air Force - 19, 99
Other DoD - MDA

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